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XTC: The XFT-TDC Mezzanine Card

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Abstract

We present evidence for documentation of the XTC, the TDC mezzanine card that forms the trigger primitives used by the XFT to find segments and then tracks. This original document was last edited in 1998, the TeX source files have been lost, and a number of facts on the ground have changed since the last modifications. However, there are still many useful and correct details, so we save the most recent version as a CDF note for posterity.

1 Introduction

The XFT-TDC mezzanine card was developed at Johns Hopkins, Argonne, and Michigan over the course of 1997-1999. I did my best to keep the documentation up to date during this time, but as so often happens, the rapid pace of events got the better of me, and I never put together a final, complete and accurate version of the document. The original intent was to make it into a CDF note, but I never did it, as I never really finished the thing. Since then, I have changed computing platforms several times, and managed to lose all the TeX source files and to keep only the output Postscript, which I have attached.

While this note still describes the basics of the card's operation pretty well, there are a number of things which are no longer correct. For instance, the expected running scenarios never materialized. We had been told that the "very slow" gas would almost certainly not be used, but in fact the maximum drift times are even longer than given for that scenario. Fortunately, the card could handle it, because it sent multiple copies of the output bits on to the Finder.

Figure 6, which shows the logic for setting prompt and delayed bits, is not the final version used on the board. Correct schematics are at `http://cdfrh0.grid.umich.edu/~bloom/xtc`.

Figure 9 has been a source of confusion to people working on the XFT upgrade. The output bits shown on the last line do not have 50% duty cycles with respect to each 132 ns CDF clock cycle; each bit is in fact high or low for a full 22 ns before the next transition.

Despite the failings of this document, I hope that it is still of use to those who continue to care for and develop the XFT.

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XTC: The COT TDC Mezzanine Card

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Note: *The most up-to-date version of this document and other information relating to the mezzanine card can be found on the web at http://tquark.pha.jhu.edu/xft/mezzanine.html.*

1 Introduction

The COT TDC mezzanine card generates the trigger primitives that are used by the eXtremely Fast Tracker (XFT) to identify tracks in the Central Outer Tracker (COT)[1]. (Since the card performs TDC functions for the XFT, it is also called the XFT TDC card, or XTC.) The nature of these primitives is indicated in Figure 1, which shows a track passing through a COT cell. The track passes close by to one or two wires and produce an early or "prompt" hit, which locates the track in r-ϕ. Other nearby wires get hit at later times and produce "delayed" hits, which carry information about the track's slope, and therefore its momentum. The XTC generates two bits of information—a prompt and a delayed bit—for each sense wire in the COT's four axial super layers. This information is used by the XFT to reconstruct tracks with the efficiency and precision required for CDF physics triggers.

The physical layout of this system is shown in Figure 2. The COT signals are received on the endplate by the Penn ASDs, which read out 2 cells (24 channels) each. The discriminated signals are sent over microcoax cables to a repeater board located just outside the endplug, where they are patched to a ribbon cable that runs to the front-end TDC crates. Each TDC card contains 96 channels and receives input from eight adjacent COT cells in a given superlayer. The XTC is a mezzanine card on the TDC card. It receives the 96 wire inputs, compares them to precision reference signals generated from CDF_CLK, and sets the prompt and delayed bits for each wire. These bits are driven off the XTC to the J3 backplane as single-ended TTL levels every 22 ns, i.e. 6 times the basic 132 ns clock rate. In addition, control bits such as a data word zero, a zero crossing marker, and a data strobe are sent. These signals are sent to a transition card that converts them to LVDS and drives them over 200-foot Ansley cables to the XFT Finder inputs in the first-floor counting room.

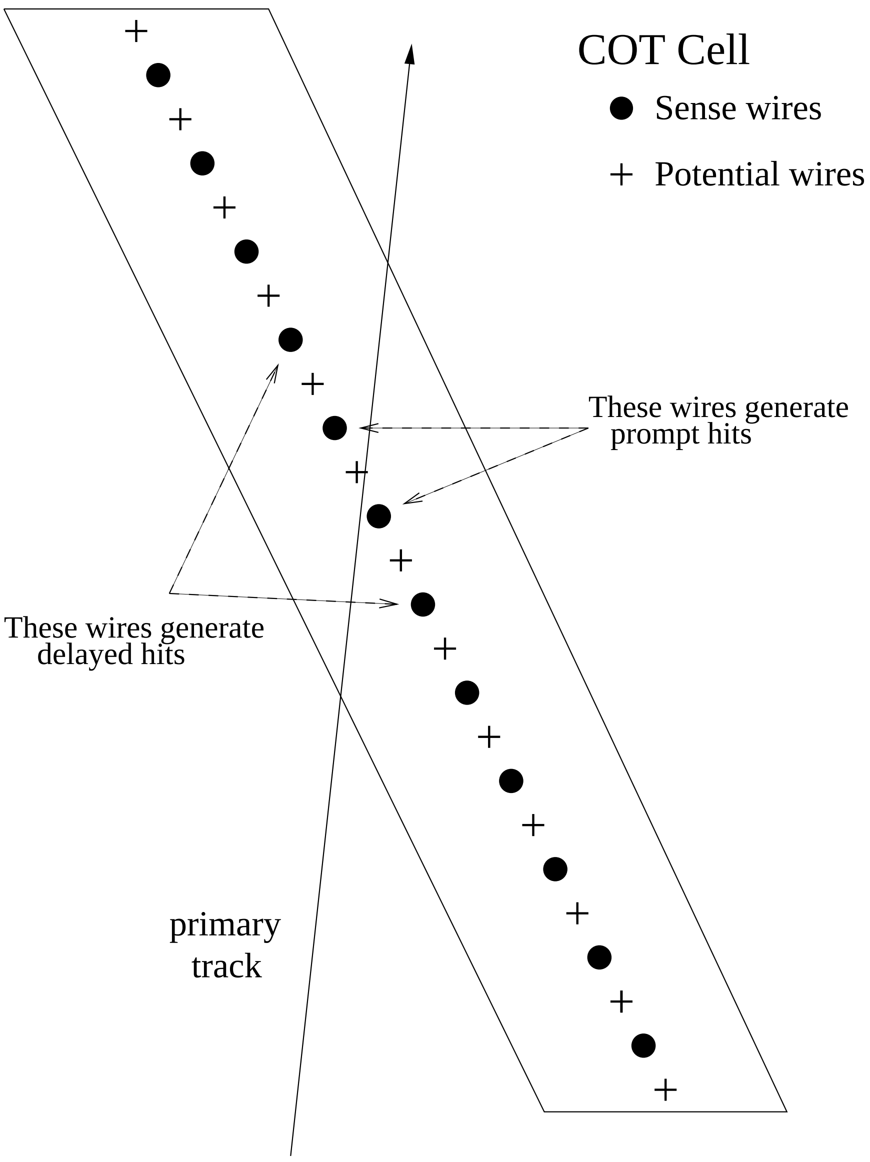

Figure 1: A charged particle passing through a COT cell, showing the resulting prompt and delayed hits.

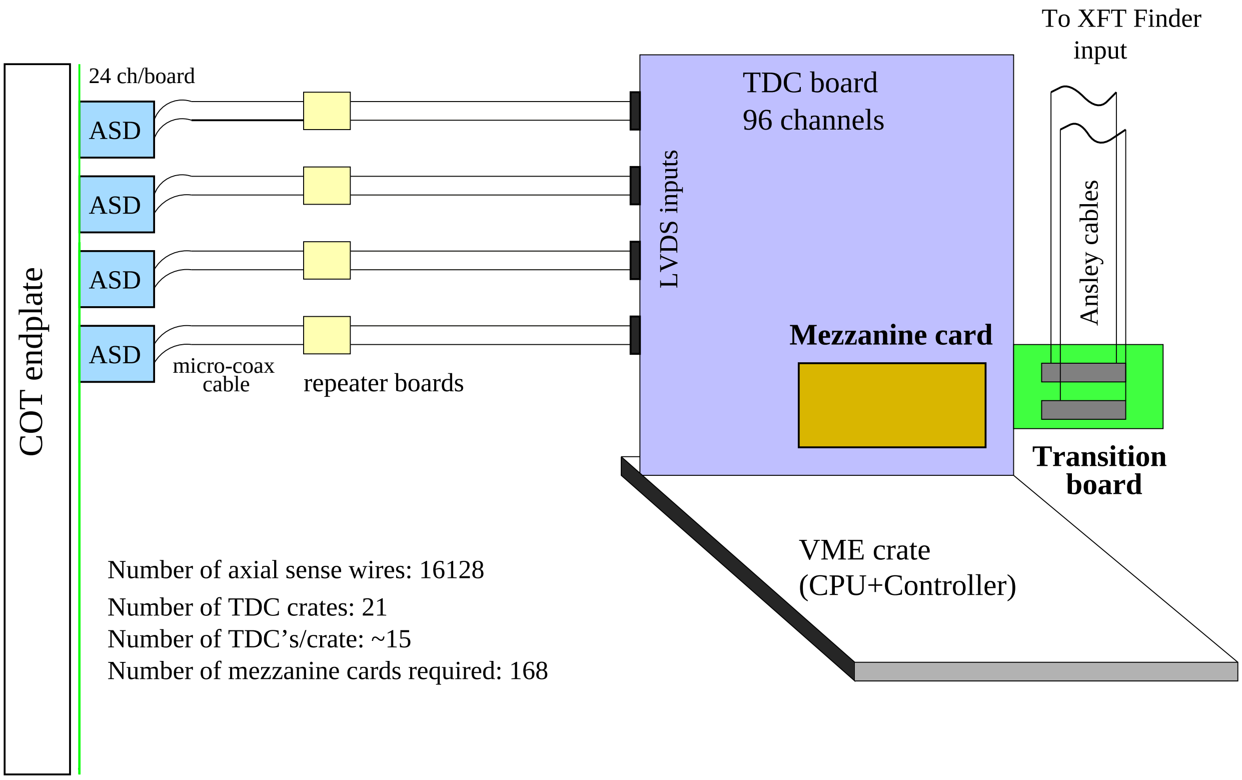

Figure 2: Physical layout of the COT readout system.

2 Timing

The COT is designed to take data with both 396 ns and 132 ns bunch crossing times. Three different gas mixtures are contemplated, each with different drift times. These differences affect the definition of the prompt and delayed windows, as well as the time at which the prompt and delayed bits can be shipped upstairs. The XTC design must be flexible enough to accommodate all of these options.

2.1 COT timing

For 132 ns operation, a "fast gas" mixture (15% CF_4) will be used that results in a maximum drift time of 111 ns. For 396 ns operation, it is possible to use slower gas mixtures. The baseline gas mixture in this mode contains 5% CF_4 ("slow gas") and has a maximum drift time of 167 ns. Running with no CF_4 in the mix, though not currently in the baseline, cannot be ruled out. This "very slow gas" option would have a maximum drift time of 196 ns. Table 1 summarizes the COT timing for the three main scenarios[2].

Beam crossing	132 ns	396 ns	396 ns
Gas mix (Ar:Et:CF_4)	50:35:15 (fast)	50:45:5 (slow)	50:50:0 (very slow)
drift velocity (μm/ns)	90	60	51
max drift time (ns)	111	167	196
nominal prompt window (ns)	44	66	66

Table 1: Summary of COT timing options.

While the CDF_CLK signal, which is the reference for the beginning of the prompt window, arrives at the TDC crates simultaneous with the beam crossing in CDF, COT signals need to propagate along the 3.2 meter length of the chamber, which takes 10 ns, and along about 66 ns of cable between the COT front end and the TDC crates. The signal propagation time thus constitutes a "t_0" that must be accounted for when creating prompt and delayed bits.

2.2 Prompt/Delayed Definition

The XTC is essentially a two-bit TDC (in the non-pejorative sense), *i.e.*, it distinguishes a prompt hit from a delayed hit. The dividing line between "prompt" and "delayed" must be optimized through simulation studies and is a function of the drift parameters of the COT gas. Studies have shown[3] that the best XFT performance is obtained when the prompt window extends to approximately the first third of the maximum drift time, i.e. about 40 ns for 132 ns operation with fast gas. The delayed window then extends from the end of the prompt window to the maximum drift time.

At first glance, it would appear that the prompt/delayed logic on the XTC should simply check if a given channel is over threshold during the prompt or delayed window and, if so, set the appropriate bit. This is almost, but not quite, the case. The width of the pulses from the ASDs is 30-40 ns, so the majority of prompt hits actually extend into the delayed window. Simulation studies indicate that it is best not to set the delayed bit in cases where it most likely results from the tail of a prompt hit. For this reason, we subdivide the delayed window two roughly equal halves, NOTSURE and LATE. The delayed bit is *not* set if the channel shows a PROMPT hit and a NOTSURE hit but not a LATE hit. Aside from this case, the delayed bit is the logical OR of NOTSURE and LATE. Table 2 shows the truth table for prompt/delayed bit-setting.

Input:	PROMPT	NOTSURE	LATE	Output:	PROMPT	DELAYED
	0	0	0		0	0
	1	0	0		1	0
	0	1	0		0	1
	0	0	1		0	1
*	1	1	0		1	0
	1	0	1		1	1
	0	1	1		0	1
	1	1	1		1	1

Table 2: Truth table for prompt/delayed bit-setting. Except in the case indicated by the asterisk, the DELAYED bit is the logical OR of NOTSURE and LATE. The PROMPT, NOTSURE, and LATE windows correspond roughly to the first, middle, and last third of the drift time respectively.

2.3 Front-End Timing and Control Signals

The XTC sets up the prompt/delayed gates and drives the output data flow to the transition board using various global timing signals that are present on the VME backplane and are made available to the mezzanine card by the TDC board. These signals include:

- CDF_CLK. The only global precision signal in CDF, this clock runs with a 132 ns period (in both 132 ns and 396 ns accelerator operation). The rising edge is simultaneous with the beam crossing time. The duty cycle is programmable in 19 ns increments. It is expected that CDF_CLK will be at a logic high for 3-4 such increments. The timing of every signal on the XTC is defined relative to the rising edge of CDF_CLK.

- CDF_BC*. This signal is a gate for CDF_CLK, and will be in a logic low state at least 10 ns before a live crossing. In 132 ns running, when every CDF_CLK indicates a live crossing, CDF_BC* might always be in a low state, except during abort gaps.

- CDF_B0*. Marker for the nominal “bunch zero” crossing. This information is used by the XFT for data alignment.

- CDF_L1A*. Indicates a Level 1 trigger accept. This is used on the XTC to save the prompt/delayed bits in on-board FIFOs that can be read back through the TDC parallel bus for diagnostic purposes. These FIFOs are not read out during regular operation.

Figure 3 shows timing diagrams for 132 ns operation, while Figure 4 shows a similar diagram for 396 ns operation.

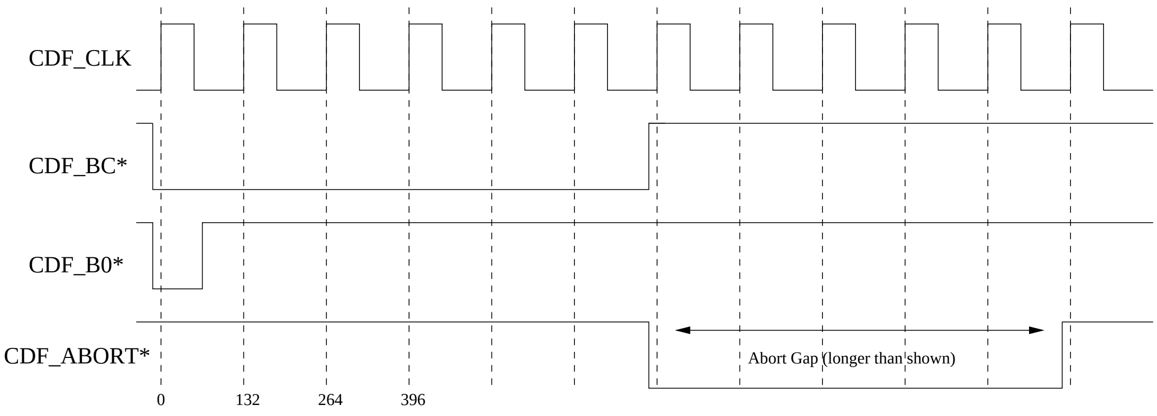

Figure 3: Front-end timing and control signals for 132 ns operation.

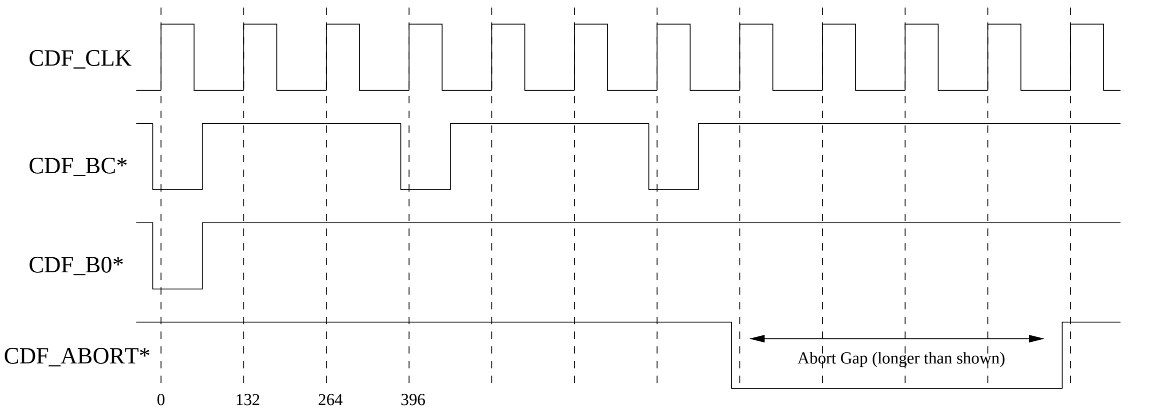

Figure 4: Front-end timing and control signals for 396 ns operation.

3 Mezzanine Card Implementation

The design of the XTC follows the guidelines specified in CDF note 4021, "Developing Mezzanine Cards"[4]. This note contains many details, not reproduced here, about general features of mezzanine card design such as the mechanical and connector specifications, Xilinx program and parameter loading, downloading setup data, power and cooling requirements, etc. A block diagram of the mezzanine card logic is shown in Figure 5.

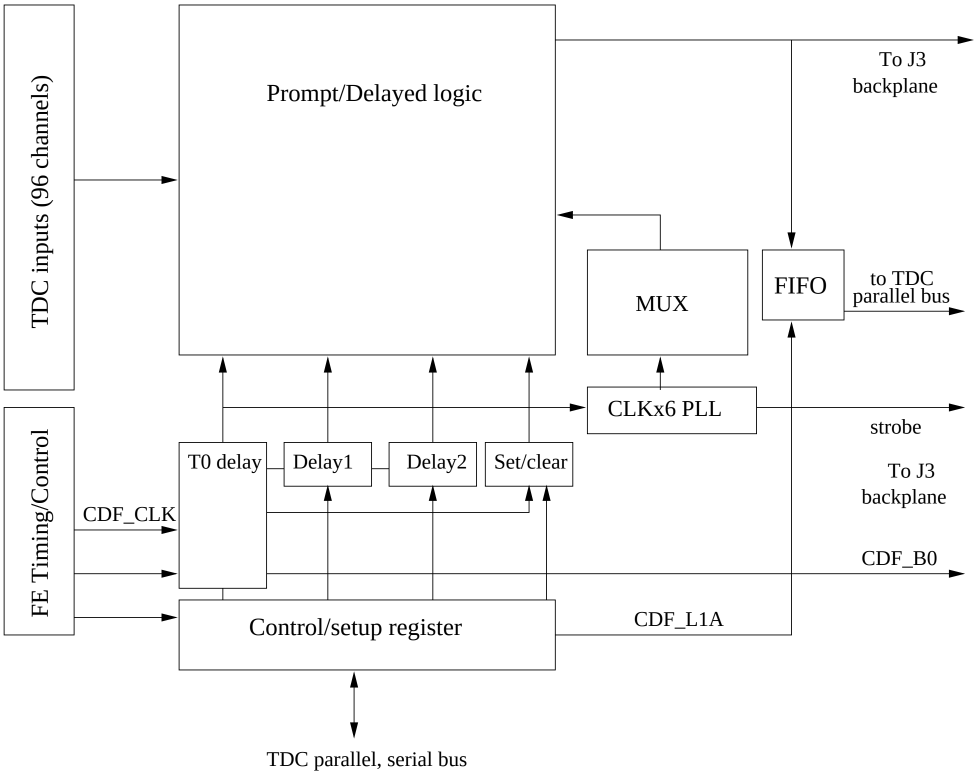

Figure 5: Block diagram of the mezzanine card logic.

3.1 Timing gates

To establish the timing gates necessary for prompt and delayed hits, the CDF_CLK signal is passed through a series of Data Delay 3D7408S programmable silicon delays. The first delay compensates for the t_0 offset due to signal propagation delay between the COT endplate and the XTC. Nominally, this delay is about 70 ns and is dominated by the cable delay from the ASD through the repeater board to the TDC card front end. The delay is adjustable in 1 ns increments at the board level to take out the effect of slewing of CDF_CLK along the TDC crate backplane. After the t_0 delay has been adjusted, the rising edge of the delayed CDF_CLK should be in synch with the earliest possible time at which valid data from the current crossing could arrive. In CDF, the value of this delay will be calibrated for each XTC.

The CDF_BC* and CDF_B0* signals are also delayed, to stay in synch with the delayed CDF_CLK. Nominally, these delays will all be the same length, but each can be set separately, also in 1 ns increments. The values for all of the delays are kept in eight-bit registers in one of the four Xilinx XC95216 CPLD chips that are on the XTC. This Xilinx will be referred to as the "kitchen sink," since it carries out a variety of tasks. The registers can be read and written over the TDC parallel bus, through the protocol described in CDF 4021. From the outside world, these registers can be read and written with standard VME reads and writes; the TDC board handles the parallel bus protocol.

The delayed CDF_CLK edge is the basis for all other signals on the card. The other signals are only created during live crossings, as indicated by CDF_BC*; otherwise, data would be overwritten in 396 ns mode, when there is more than one CDF_CLK edge per live crossing. The delayed CDF_CLK is piped through another programmable delay, Delay1, and its output defines the end of the PROMPT window. This output is also passed through a second programmable delay, Delay2, which defines the end of the NOTSURE window. The delays are adjustable in 1 ns increments, and their values are stored in the kitchen sink. The nominal values are the nominal widths of the PROMPT and NOTSURE windows, each 44 ns in 132 ns operation. The kitchen sink uses these delayed clock edges to create signals that are in a logic high state during the various timing windows; these are the actual timing gates.

The delayed CDF_CLK is also piped to two other programmable delays, which are used to create the set and clear the bits within the TDC circuit, as described below. There are separately adjustable delays in 1 ns increments for the prompt and delayed bits, so that the prompt bits can be finalized and multiplexed out while delayed data is still arriving in 396 ns operation. These values are also set in the kitchen sink registers. For 132 ns operation, the prompt and delayed set/clear signals will come about 70 ns and 140 ns, respectively, after the delayed CDF_CLK edge; the signals cannot be set until data from the previous crossing has been sent to the backplane.

3.2 TDC logic

Precise timing of the XTC signals is critical for the proper performance of the XFT. A design goal of this board is to keep the channel-to-channel timing variation less than 5 ns. This goal motivates the desire to implement the prompt/delayed logic in the Xilinx XC9500 CPLD

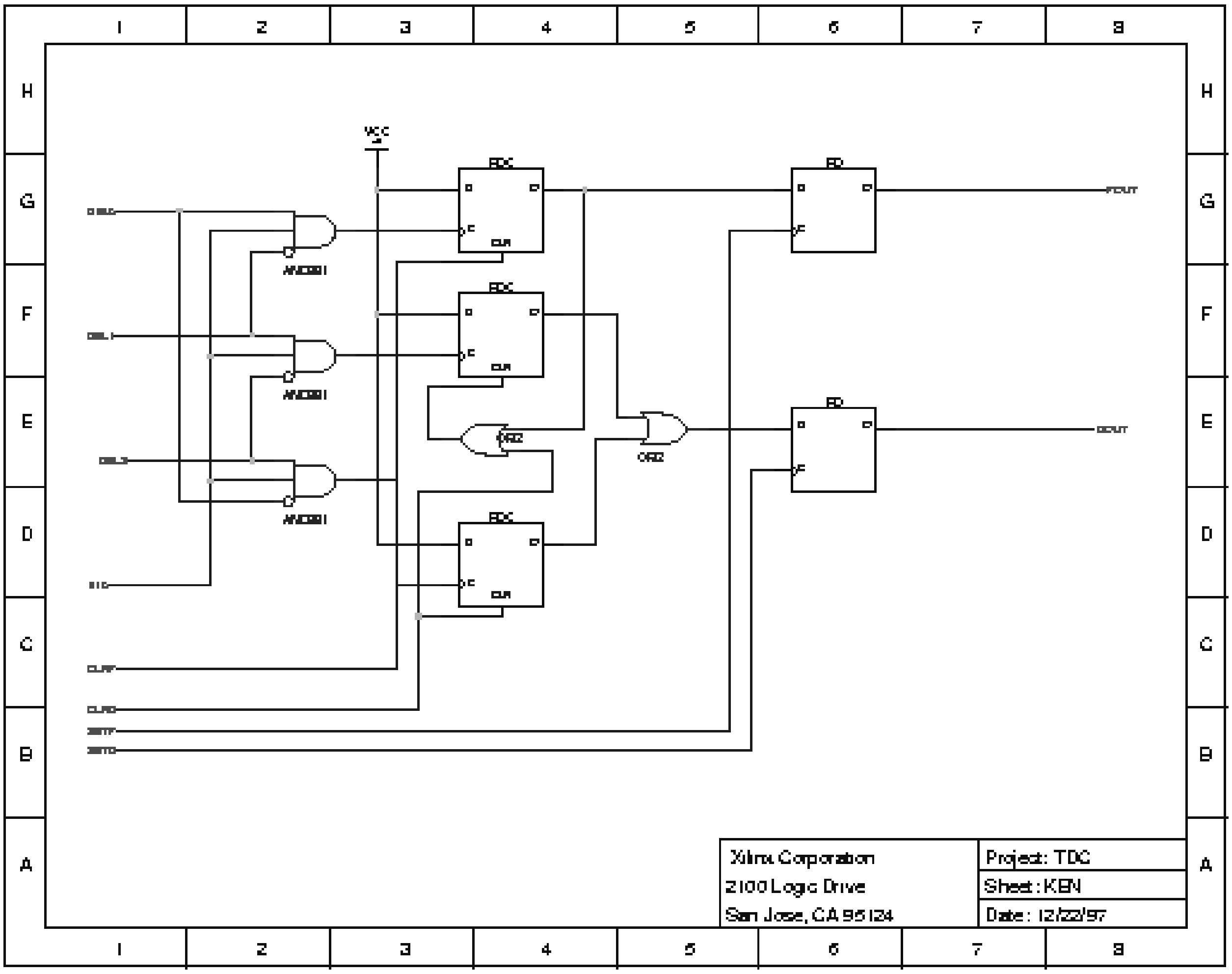

Figure 6: Xilinx implementation of prompt/delayed bit-setting logic.

chipset, a series known for excellent channel-to-channel timing stability.

The prompt/delayed logic section receives the 96 wire inputs and uses the timing gates set as described above to implement the truth table of Table 2. The logic for a single channel is shown in Figure 6. Signals common to all channels, such as the timing gates, are created in the kitchen sink and fanned out to the individual wire channels located in the TDC CPLDs. The three DEL signals are the PROMPT, NOTSURE, and LATE timing gates. Their status is compared to the input signal from the COT, and the resulting ANDs are registered in flip-flops. The NOTSURE and LATE outputs or ORed together, but the NOTSURE flip-flop is disabled when the prompt bit is set, enforcing the truth table in Table 2. The set signals save resulting prompt and delayed bits on another pair of flip-flops. While separate set and clear signals are indicated, the same pulse can and will be used to store the output bits, and to clear the initial set of flip-flops.

Three Xilinx chips on the XTC carry out the TDC logic; each one processes 32 channels of COT data. Our tests indicate that signal propagation times for the different channels within one chip vary by less than 1.5 ns.

3.3 Phase-locked loop

The output of the t_0 delay stage of CDF_CLK is also used as input to phase-locked loop that generates an output signals of six times the input frequency. The CDF_CLK*6 (22 ns) signal is used to multiplex the prompt/delayed bits. The phase-locked loop chip is a Motorola MC88915, and the kitchen sink Xilinx is used to count down to achieve the right frequency multiple. The phase of the CDF_CLK*6 signal with with respect to the delayed CDF_CLK signal is controlled programmable delays placed before the phase-locked loop input and after the output that are adjustable in 0.5 ns and 0.25 ns steps, respectively. The delay values are kept in the kitchen sink registers.

3.4 Output multiplexing

Prompt/delayed bits are sent to the transition board in six 22 ns cycles beginning with the next (t_0-delayed) CDF_CLK after the current crossing. Timing diagrams for 132 and 396 ns operation are shown in Figures 7-9. In 396 ns operation, the delayed window extends beyond 132 ns, i.e. into the next CDF_CLK. By using CDF_BC to determine live crossings, and adjusting the times of the prompt and delayed set and clear signals, the XTC can be configured for 132 ns or 396 ns operation.

Each transition board drives two Ansley cables, each with 25 signal pairs. A total of 192 data bits must be sent (a prompt and a delayed bit for each of the 96 wires), which can be handled with (2 Ansleys)$\times$(6 data cycles)$\times$(16 bits per Ansley per cycle). In each data cycle, the 32 bits sent on the two Ansley cables come from a single Xilinx TDC chip. The kitchen sink chip has a counter that is incremented with each CDF_CLK*6 clock cycle, and this counter selects six different output enable signals. Each enable signal tells a different TDC chip to put either its 32 prompt bits or its 32 delayed bits onto the 32 available data output lines.

On each cycle, we send to each Ansley the 16 data bits, a data strobe, a data word zero marker, and a CDF_B0 marker if appropriate. The prompt bits are sent on the first three cycles and the delayed bits on the last three. This protocol is shown in Table 3. The data strobe runs continuously and is coincident with the data; it is generated by ORing the zeroth, second, and fourth enable signals. The word zero bit is generated from the zeroth enable, and also runs continuously. CDF_B0 is set for all six words of a "beam zero" event. The multiplexing scheme requires that wires 0-15 and 48-63 all be processed on one TDC chip, wires 16-31 and 64-79 on the second, and wires 32-47 and 80-95 on the third.

3.5 Channel map

The wire numbers specified in Table 3 are given in the XFT wire numbering scheme. This is illustrated in Figure 10, along with the TDC board channel numbers associated with each wire. TDC channel numbers increase first in r, and then in cell number, or ϕ. In constrast, XFT wire numbers increase first in ϕ and then in r, with a break occurring in the middle of the two sub-blocks of four cells; each sub-block's data is sent on a different Ansley. The

Pairs 1,2	Pair 3	Pair 4	Pair 5	Pair 6	Pair 7	Pairs 8-23	Pairs 24,25
GND	STROBE	GND	B0	GND	logic high	Wr. 0-15 P	GND
GND	STROBE	GND	B0	GND	logic low	Wr. 16-31 P	GND
GND	STROBE	GND	B0	GND	logic low	Wr. 32-47 P	GND
GND	STROBE	GND	B0	GND	logic low	Wr. 0-15 D	GND
GND	STROBE	GND	B0	GND	logic low	Wr. 16-31 D	GND
GND	STROBE	GND	B0	GND	logic low	Wr. 32-47 D	GND

Table 3: XTC-to-Finder protocol for the first Ansley. The second Ansley handles channels 48-95. The rows of the table represent successive 22 ns clock cycles. The wire numbers are in the XFT number scheme.

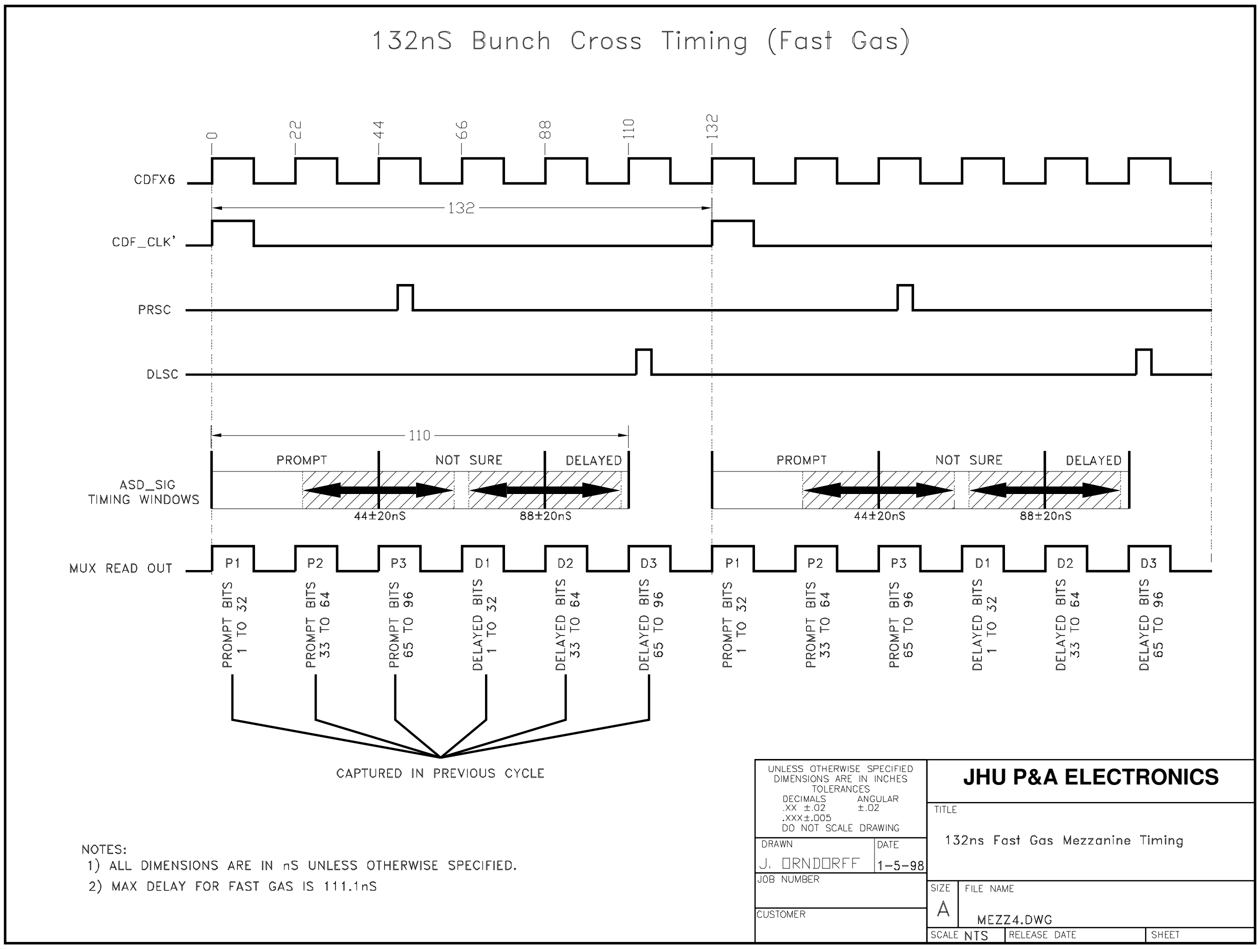

Figure 7: Prompt/delayed timing diagram for 132 ns operation, showing the expected PROMPT, NOTSURE, and LATE windows and the multiplexing scheme.

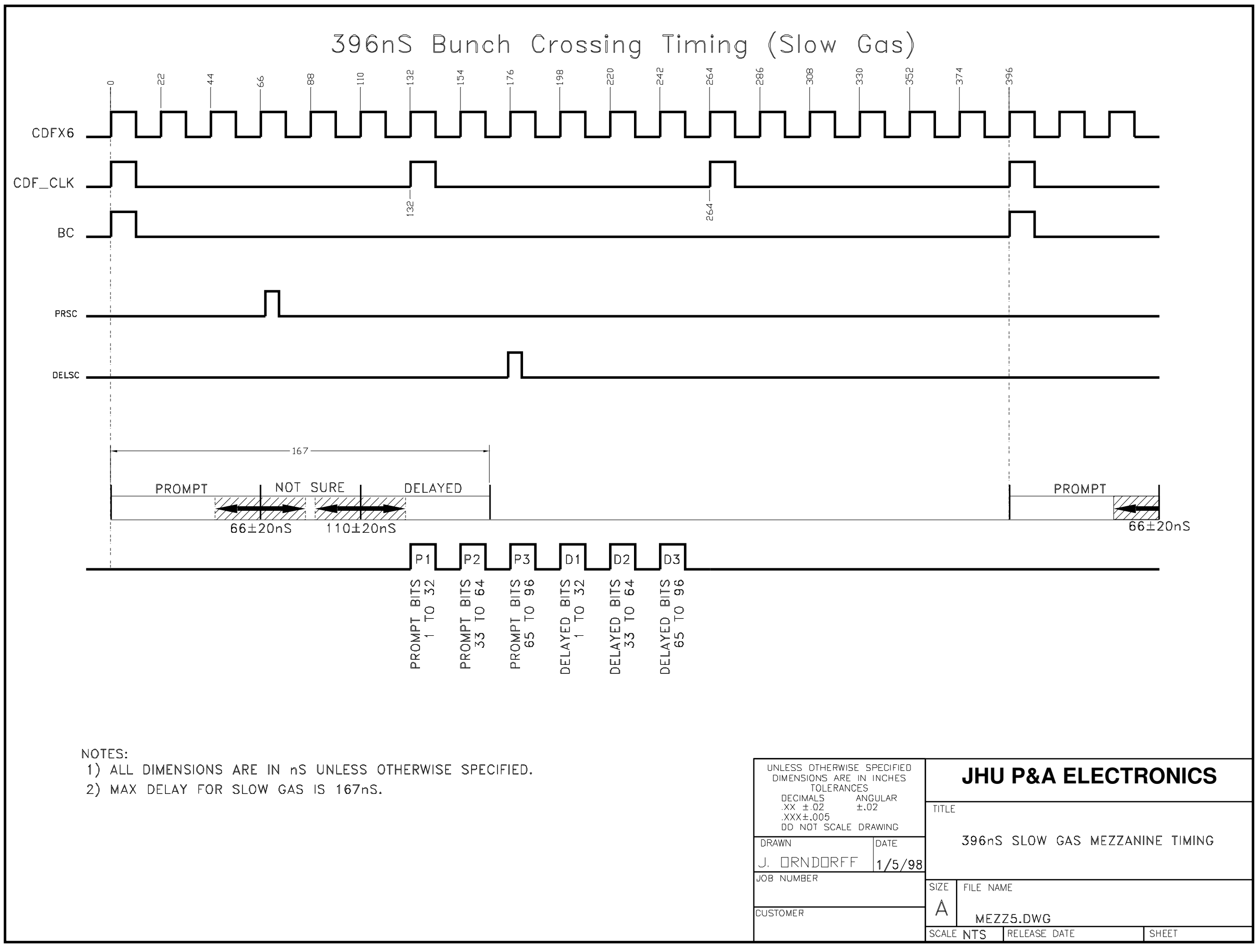

Figure 8: Prompt/delayed timing diagram for 396 ns operation with slow gas, showing the expected PROMPT, NOTSURE, and LATE windows and the multiplexing scheme.

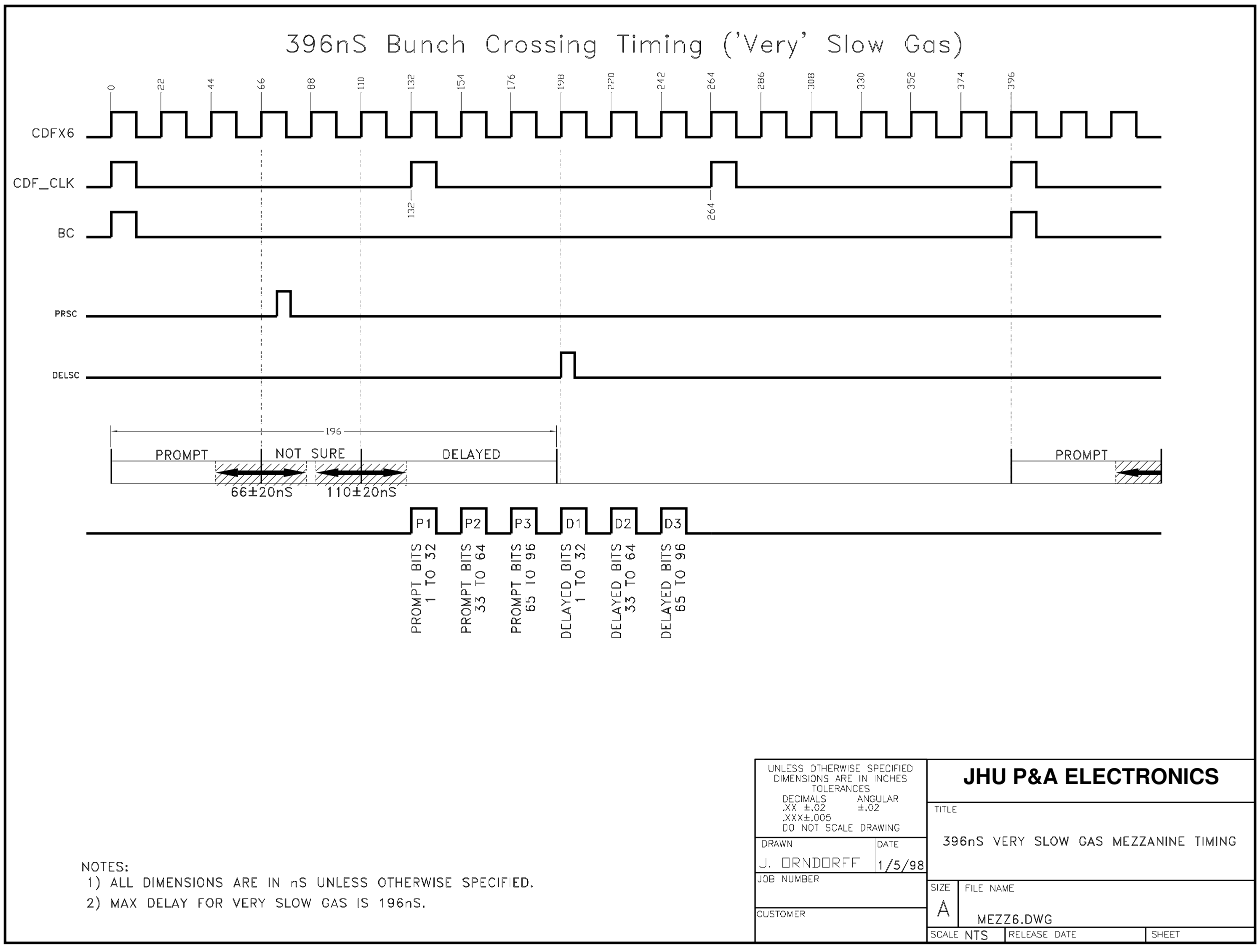

Figure 9: Prompt/delayed timing diagram for 396 ns operation with "really slow" (no CF_4) gas, showing the expected PROMPT, NOTSURE, and LATE windows and the multiplexing scheme.

mapping of TDC channels to XFT wire numbers takes place within the Xilinx TDC chips; due to the constraints of Xilinx programming, it is not clear if the map can be changed in the Xilinx alone without modifications to the printed circuit boards.

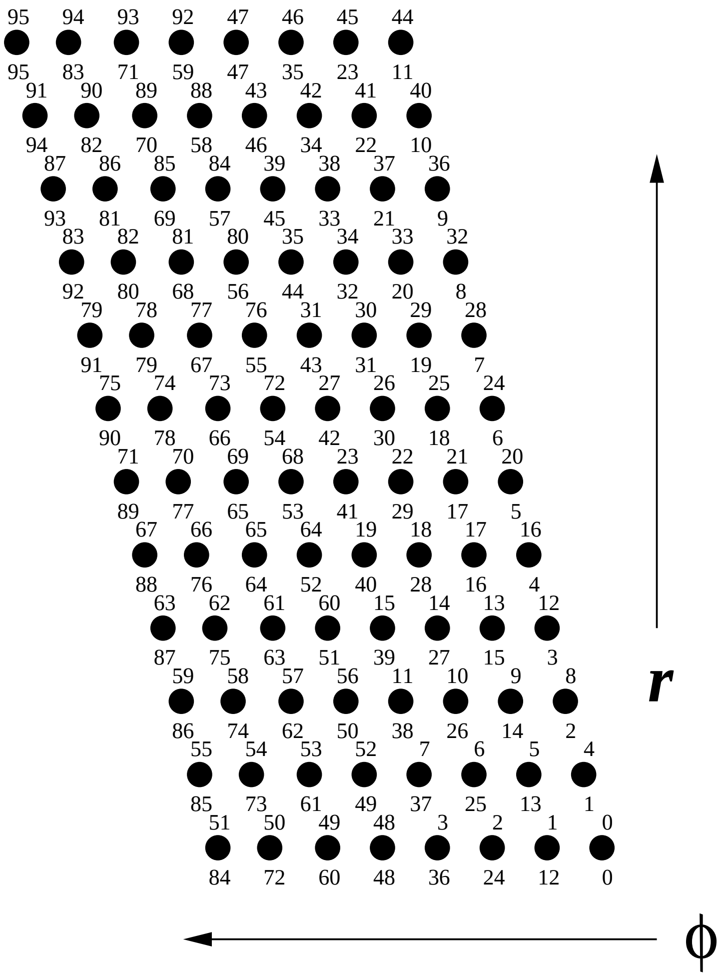

Figure 10: Wire numbering schemes. The XFT wire numbers are shown above the dots that represent the wires, and the TDC channel numbers below.

3.6 Diagnostic latch

A final feature is a data latch that holds TDC chip output, which is used for diagnostic purposes only. The latch consists of a group of four Cypress CY7C433 FIFOs, each eight bits wide and 1024 entries deep. When a CDF_L1A signal comes in coincidence with a set of data, the resulting prompt and delayed bits are stored in the FIFOs. On each of the six data writeout cycles, the active Xilinx sends its 32 bits into the four FIFOs. The FIFOs can be read out (in succession) over the TDC parallel bus. A total of 24 FIFO reads provides all 192 prompt and delayed bits.

4 Performance So Far

As of June 1998, four prototype XTCs have been built. They all perform as they were designed. The TDC calibration feature of the Tracer board is used to put input pulses on the backplane. These pulses are fanned out by the TDC board to the 96 channels on the XTC. We have observed the correct prompt and delayed bits for given input pulses. The logic of the NOTSURE window is implemented correctly. Output bits have been observed both at the back end of the TDC boards, and in the XTC FIFOs when L1A signals are sent.

A single XTC, mounted to a TDC card, has been used in conjunction with a pair of Ansley cables and an XFT Finder board. The Tracer pulses were used to generate prompt and delayed bits on specified channels, and these were successfully captured by the Finder. Most recently, the Finder has been able to set a pixel for a found segment based on a pattern sent by the XTC card.

One issue that has been raised recently is the relative skew of the XTC output bits. Over the length of the Ansley cables, the signals sent by the XTC get distorted, and the data valid window at the Finder input is closer to 12 ns than 22 ns. As a result, the skew should be kept as small as possible to keep bits from being lost. The Finder design team has requested that the skew be less than 1 ns for all data bits. At the moment, the average skew of data bits from the strobe is about 0.7 ns, but some bits are as far as 2 ns away. To remedy this, we will replace the XTC output buffers with a low-skew latch in our next (and presumably final) prototype. However, we have demonstrated that the Finder works just fine with the current level of skew, so we don't expect this to be a problem in the final system.

A XTC Memory Map

All XTC memory addresses can be treated just like standard VME addresses; communication with the mezzanine card across the TDC parallel bus is handled by a PAL on the TDC board. In the TDC memory map, all mezzanine card addresses start at 0x2041C00. The XTC memory map is given in Table 4.

References

[1] The XFT and COT are described in detail in the CDF II Detector Technical Design Report, Fermilab-Pub-96/390-E, Nov. 1996. The XFT group's web page is available at http://www-cdf.fnal.gov/internal/upgrades/daq_trig/xft_home.html.

[2] Kevin Pitts, private communication, 9/17/96.

[3] Reference to R. Hughes et al. simulation studies to define prompt/delayed windows.

[4] M. Campbell *et al.*, "Developing Mezzanine Cards," CDF note 4021, Revision B, Feb. 1997.

Address	Bit	Function
2041C00		CDF_CLK Delay (1 ns/step) (r/w)
2041C04		CDF_BC Delay (1 ns/step) (r/w)
2041C08		PLL Input Delay (0.5 ns/step) (r/w)
2041C0C		PLL Output Delay (0.25 ns/step) (r/w)
2041C10		CDF_B0 Delay (1 ns/step) (r/w)
2041C14		Clock 1 Delay (end of PROMPT) (1 ns/step) (r/w)
2041C18		Clock 2 Delay (end of NOTSURE) (1 ns/step) (r/w)
2041C1C		Prompt Set/Clear Delay (1 ns/step) (r/w)
2041C20		Delayed Set/Clear Delay (1 ns/step) (r/w)
2041C24		FIFO Status (r)
	0	FIFO 0 Empty
	1	FIFO 1 Empty
	2	FIFO 2 Empty
	3	FIFO 3 Empty
	4	FIFO 0 Full
	5	FIFO 1 Full
	6	FIFO 2 Full
	7	FIFO 3 Full
2041C28		FIFO Clear (w)
2041C30		FIFO 0 Contents (r)
2041C34		FIFO 1 Contents (r)
2041C38		FIFO 2 Contents (r)
2041C3C		FIFO 3 Contents (r)

Table 4: XTC Memory Map