Pulsar Firmware for L2 trigger upgrade

Appendix 1:

VME address maps

FIFO and DAQ RAM sizes

Muon VME addresses

DataIO FPGA 1

Name	Address	Description	Databits	Data
Firmware version	YY080000 **(R)**	Firmware version	31…0	0x08407020
Reset	YY080004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY080008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY08000C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 1	YY080010 **(R)**	Not used	31…0	0x00c0ffee
Pulse 1	YY080014 **(W)**	Not used	-	-
Control register 2	YY080018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY08001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY080020 **(R)**	Not used	31…0	0x00000cdf

DataIO FPGA 2

Name	Address	Description	Databits	Data
Firmware version	YY0C0000 **(R)**	Firmware version	31…0	0x08407020
Reset	YY0C0004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY0C0008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY0C000C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 1	YY0C0010 **(R)**	Not used	31…0	0x00c0ffee
Pulse 1	YY0C0014 **(W)**	Not used	-	-
Control register 2	YY0C0018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY0C001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY0C0020 **(R)**	Not used	31…0	0x00000cdf

Control FPGA

Name	Address	Description	Databits	Data
Firmware version	YY000000 **(R)**	Firmware version	31…0	0x04408060
Reset	YY000004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY000008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY00000C **(R/W)**	Bunch Count Shift	7…0	Power-up value: 41
Status register 1	YY000010 **(R)**	Not used	31…0	0x00c0ffee
Pulse 1	YY000014 **(W)**	Not used	-	-
Control register 2	YY000018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY00001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY000020 **(R)**	Not used	31…0	0xdeadbeef
IDPROM	YY100000 – YY10007C **(R)**	IDPROM	31…24	

IDPROM

YY100000	0	YY10003C	
YY100004	0	YY100040	M
YY100008	x	YY100044	U
YY10000C	x	YY100048	O
YY100010		YY10004C	N
YY100014	0	YY100050	
YY100018	8	YY100054	R
YY10001C	6	YY100058	X
YY100020		YY10005C	
YY100024	P	YY100060	
YY100028	U	YY100064	
YY10002C	L	YY100068	
YY100030	S	YY10006C	
YY100034	A	YY100070	
YY100038	R	YY100074	
		YY100078	
		YY10007C	

ShowerMax VME addresses

DataIO FPGA 1

Name	Address	Description	Databits	Data
Firmware version	YY080000 **(R)**	Firmware version	31…0	0x08412011
Reset	YY080004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY080008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY08000C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 1	YY080010 **(R)**	Not used	31…0	0x10c0ffee
Pulse 1	YY080014 **(W)**	Not used	-	-
Control register 2	YY080018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY08001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY080020 **(R)**	Not used	31…0	0xabcdef01

DataIO FPGA 2

Name	Address	Description	Databits	Data
Firmware version	YY0C0000 **(R)**	Firmware version	31…0	0x08412011
Reset	YY0C0004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY0C0008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY0C000C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 1	YY0C0010 **(R)**	Not used	31…0	0x10c0ffee
Pulse 1	YY0C0014 **(W)**	Not used	-	-
Control register 2	YY0C0018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY0C001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY0C0020 **(R)**	Not used	31…0	0xabcdef01

Control FPGA

Name	Address	Description	Databits	Data
Firmware version	YY000000 **(R)**	Firmware version	31…0	0x0c508110
Reset	YY000004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY000008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY00000C **(R/W)**	Bunch Count Shift	7…0	Power-up value: 41
Status register 1	YY000010 **(R)**	Not used	31…0	0x00c0ffee
Pulse 1	YY000014 **(W)**	Not used	-	-
Control register 2	YY000018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY00001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY000020 **(R)**	Not used	31…0	0xdeadbeef
IDPROM	YY100000 – YY10007C **(R)**	IDPROM	31…24	

IDPROM

YY100000	0	YY10003C	
YY100004	0	YY100040	X
YY100008	x	YY100044	F
YY10000C	x	YY100048	T
YY100010		YY10004C	
YY100014	1	YY100050	R
YY100018	0	YY100054	X
YY10001C	2	YY100058	
YY100020		YY10005C	
YY100024	P	YY100060	
YY100028	U	YY100064	
YY10002C	L	YY100068	
YY100030	S	YY10006C	
YY100034	A	YY100070	
YY100038	R	YY100074	
		YY100078	
		YY10007C	

SVT VME addresses

Control FPGA

Name	Address	Description	Databits	Data
Firmware version	YY000000 **(R)**	Firmware version	31…0	0x05411100
Reset	YY000004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY000008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY00000C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 1	YY000010 **(R)**	Not used	31…0	0x00c0ffee
Pulse 1	YY000014 **(W)**	Not used	-	-
Control register 2	YY000018 **(R/W)**	RW enable	0	Power-up value: 0
Control register 3	YY00001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY000020 **(R)**	Not used	31…0	0xdeadbeef
IDPROM	YY100000 – YY10007C **(R)**	IDPROM	31…24	

IDPROM

YY100000	0	YY10003C	
YY100004	0	YY100040	S
YY100008	x	YY100044	V
YY10000C	x	YY100048	T
YY100010		YY10004C	
YY100014	0	YY100050	R
YY100018	9	YY100054	X
YY10001C	2	YY100058	
YY100020		YY10005C	
YY100024	P	YY100060	
YY100028	U	YY100064	
YY10002C	L	YY100068	
YY100030	S	YY10006C	
YY100034	A	YY100070	
YY100038	R	YY100074	
		YY100078	
		YY10007C	

CLUSTER VME addresses

DataIO FPGA 1 (ISOLIST)

Name	Address	Description	Databits	Data
Firmware version	YY080000 **(R)**	Firmware version	31…0	0x07411200
Reset	YY080004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY080008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY00000C **(R/W)**	Bunch Count Shift	7…0	Power-up value: 41
Status register 1	YY080010 **(R)**	Not used	31…0	0xffc0ffee
Pulse 1	YY080014 **(W)**	Not used	-	-
Control register 2	YY080018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY08001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY080020 **(R)**	Not used	31…0	0xdeadbeef

DataIO FPGA 2 (CLIST)

Name	Address	Description	Databits	Data
Firmware version	YY0C0000 **(R)**	Firmware version	31…0	0x06411220
Reset	YY0C0004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY0C0008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY00000C **(R/W)**	Bunch Count Shift	7…0	Power-up value: 41
Status register 1	YY0C0010 **(R)**	Not used	31…0	0xffc0ffee
Pulse 1	YY0C0014 **(W)**	Not used	-	-
Control register 2	YY0C0018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY0C001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY0C0020 **(R)**	Not used	31…0	0xdeadbeef

Control FPGA

Name	Address	Description	Databits	Data
Firmware version	YY000000 **(R)**	Firmware version	31…0	0x0B411100
Reset	YY000004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY000008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY00000C **(R/W)**	Bunch Count Shift	7…0	Power-up value: 41
Status register 1	YY000010 **(R)**	Not used	31…0	0x00c0ffee
Pulse 1	YY000014 **(W)**	Not used	-	-
Control register 2	YY000018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY00001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY000020 **(R)**	Not used	31…0	0xdeadbeef
IDPROM	YY100000 – YY10007C **(R)**	IDPROM	31…24	

IDPROM

YY100000	0	YY10003C	
YY100004	0	YY100040	C
YY100008	x	YY100044	L
YY10000C	x	YY100048	U
YY100010		YY10004C	S
YY100014	0	YY100050	T
YY100018	9	YY100054	E
YY10001C	0	YY100058	R
YY100020		YY10005C	
YY100024	P	YY100060	R
YY100028	U	YY100064	X
YY10002C	L	YY100068	
YY100030	S	YY10006C	
YY100034	A	YY100070	
YY100038	R	YY100074	
		YY100078	
		YY10007C	

TS interface VME addresses

DataIO FPGA 1

Name	Address	Description	Databits	Data
Firmware version	YY080000 **(R)**	Firmware version	31…0	0x09408210
Reset	YY080004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY080008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY08000C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 1	YY080010 **(R)**	Not used	31…0	0x02c0ffee
Pulse 1	YY080014 **(W)**	Not used	-	-
Control register 2	YY080018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY08001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY080020 **(R)**	Not used	31…0	0xdeadbeef

Control FPGA

Name	Address	Description	Databits	Data
Firmware version	YY000000 **(R)**	Firmware version	31…0	0x0A411030
Reset	YY000004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY000008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY00000C **(R/W)**	Bunch Count Shift	7…0	Power-up value: 41
Status register 1	YY000010 **(R)**	Not used	31…0	0xffc0ffee
Pulse 1	YY000014 **(W)**	Not used	-	-
Control register 2	YY000018 **(R/W)**	Not used	31…0	-
Control register 3	YY00001C **(R/W)**	Decision selection	0	Power-up value: 0 (Slink decision)
Status register 2	YY000020 **(R)**	Not used	31…0	0xdeadbeef
Control register 4	YY000028 **(R/W)**	L2 to TS delay	10…0	Power-up value: 0 (No delay)
IDPROM	YY100000 – YY10007C **(R)**	IDPROM	31…24	

IDPROM

YY100000	0	YY10003C	
YY100004	0	YY100040	T
YY100008	x	YY100044	S
YY10000C	x	YY100048	
YY100010		YY10004C	I
YY100014	0	YY100050	N
YY100018	9	YY100054	T
YY10001C	6	YY100058	E
YY100020		YY10005C	R
YY100024	P	YY100060	F
YY100028	U	YY100064	A
YY10002C	L	YY100068	C
YY100030	S	YY10006C	E
YY100034	A	YY100070	
YY100038	R	YY100074	
		YY100078	
		YY10007C	

Decision selection
YY00001C
Bit 0:
Low = Slink decision
High = L1T decision

L2 to TS delay
YY000028
Bits 10..0:
Number of SlinkCLKs (40Mhz = 25ns/clk)

Delay from decision received to sending decision to TS.

Slink merger VME addresses

DataIO FPGA 1

Name	Address	Description	Databits	Data
Firmware version	YY080000 **(R)**	Firmware version	31…0	0x01408210
Reset	YY080004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY080008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY08000C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 1	YY080010 **(R)**	Not used	31…0	0x01c0ffee
Pulse 1	YY080014 **(W)**	Not used	-	-
Control register 2	YY080018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY08001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY080020 **(R)**	Not used	31…0	0xdeadbeeb

DataIO FPGA 2

Name	Address	Description	Databits	Data
Firmware version	YY0C0000 **(R)**	Firmware version	31…0	0x01408210
Reset	YY0C0004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY0C0008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY0C000C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 1	YY0C0010 **(R)**	Not used	31…0	0x01c0ffee
Pulse 1	YY0C0014 **(W)**	Not used	-	-
Control register 2	YY0C0018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY0C001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY0C0020 **(R)**	Not used	31…0	0xdeadbeeb

Control FPGA

Name	Address	Description	Databits	Data
Firmware version	YY000000 **(R)**	Firmware version	31…0	0x02411290
Reset	YY000004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY000008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY00000C **(R/W)**	Bunch Count Shift	7…0	Power-up value: 41
Status register 1	YY000010 **(R)**	Not used	31…0	0x00c0ffee
Pulse 1	YY000014 **(W)**	Not used	-	-
Control register 2	YY000018 **(R/W)**	Input selection	3…0	Power-up value: 8 (4th disabled)
Control register 3	YY00001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY000020 **(R)**	Not used	31…0	0xdeadbeef
IDPROM	YY100000 – YY10007C **(R)**	IDPROM	31…24	

IDPROM

YY100000	0	YY10003C	
YY100004	0	YY100040	S
YY100008	x	YY100044	L
YY10000C	x	YY100048	I
YY100010		YY10004C	N
YY100014	0	YY100050	K
YY100018	9	YY100054	
YY10001C	4	YY100058	M
YY100020		YY10005C	E
YY100024	P	YY100060	R
YY100028	U	YY100064	G
YY10002C	L	YY100068	E
YY100030	S	YY10006C	R
YY100034	A	YY100070	
YY100038	R	YY100074	
		YY100078	
		YY10007C	

Input selection
YY000018
Bit 0: Input 1
Bit 1: Input 2
Bit 2: Input 3
Bit 3: Input 4
High = disable
Low = enable
Power-up = Input 4 disabled

XFT VME addresses

DataIO FPGA 1

Name	Address	Description	Databits	Data
Firmware version	YY080000 **(R)**	Firmware version	31…0	0x0d509190
Reset	YY080004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY080008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY08000C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 1	YY080010 **(R)**	Not used	31…0	0x00c0ffee
Pulse 1	YY080014 **(W)**	Not used	-	-
Control register 2	YY080018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY08001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY080020 **(R)**	Not used	31…0	0x00000cdf

DataIO FPGA 2

Name	Address	Description	Databits	Data
Firmware version	YY0C0000 **(R)**	Firmware version	31…0	0x0d509190
Reset	YY0C0004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY0C0008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY0C000C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 1	YY0C0010 **(R)**	Not used	31…0	0x00c0ffee
Pulse 1	YY0C0014 **(W)**	Not used	-	-
Control register 2	YY0C0018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY0C001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY0C0020 **(R)**	Not used	31…0	0x00000cdf

Control FPGA

Name	Address	Description	Databits	Data
Firmware version	YY000000 **(R)**	Firmware version	31…0	0x0c508110
Reset	YY000004 **(W)**	Reset FPGA	-	-
DAQ SW version	YY000008 **(R/W)**	DAQ SW version	31…0	Power-up value: 0
Control register 1	YY00000C **(R/W)**	Bunch Count Shift	7…0	Power-up value: 41
Status register 1	YY000010 **(R)**	Not used	31…0	0x00c0ffee
Pulse 1	YY000014 **(W)**	Not used	-	-
Control register 2	YY000018 **(R/W)**	Not used	31…0	Power-up value: 0
Control register 3	YY00001C **(R/W)**	Not used	31…0	Power-up value: 0
Status register 2	YY000020 **(R)**	Not used	31…0	0xdeadbeef
IDPROM	YY100000 – YY10007C **(R)**	IDPROM	31…24	

IDPROM

YY100000	0	YY10003C	
YY100004	0	YY100040	X
YY100008	x	YY100044	F
YY10000C	x	YY100048	T
YY100010		YY10004C	
YY100014	1	YY100050	R
YY100018	0	YY100054	X
YY10001C	5	YY100058	
YY100020		YY10005C	
YY100024	P	YY100060	
YY100028	U	YY100064	
YY10002C	L	YY100068	
YY100030	S	YY10006C	
YY100034	A	YY100070	
YY100038	R	YY100074	
		YY100078	
		YY10007C	

DataIO1 DAQ readout

Word count registers

Mezzanine card 1		Mezzanine card 2	
Channel 1		**Channel 1**	
Buffer 0	XX080800	Buffer 0	XX08080C
Buffer 1	XX080900	Buffer 1	XX08090C
Buffer 2	XX080A00	Buffer 2	XX080A0C
Buffer 3	XX080B00	Buffer 3	XX080B0C
Channel 2		**Channel 2**	
Buffer 0	XX080804	Buffer 0	XX080810
Buffer 1	XX080904	Buffer 1	XX080910
Buffer 2	XX080A04	Buffer 2	XX080A10
Buffer 3	XX080B04	Buffer 3	XX080B10
Channel 3		**Channel 3**	
Buffer 0	XX080808	Buffer 0	XX080814
Buffer 1	XX080908	Buffer 1	XX080914
Buffer 2	XX080A08	Buffer 2	XX080A14
Buffer 3	XX080B08	Buffer 3	XX080B14

RAM Read VME addresses

Mezzanine card 1		Mezzanine card 2	
Channel 1		**Channel 1**	
Buffer 0	XX880000-XX8801FC	Buffer 0	XX880800-XX88097C
Buffer 1	XX980000-XX9801FC	Buffer 1	XX980800-XX98097C
Buffer 2	XXA80000-XXA801FC	Buffer 2	XXA80800-XXA8097C
Buffer 3	XXB80000-XXB801FC	Buffer 3	XXB80800-XXB8097C
Channel 2		**Channel 2**	
Buffer 0	XX880200-XX883FC	Buffer 0	XX880A00-XX880BFC
Buffer 1	XX980200-XX9803FC	Buffer 1	XX980A00-XX980BFC
Buffer 2	XXA80200-XXA803FC	Buffer 2	XXA80A00-XXA80BFC
Buffer 3	XXB80200-XXB803FC	Buffer 3	XXB80A00-XXB80BFC
Channel 3		**Channel 3**	
Buffer 0	XX880400-XX8805FC	Buffer 0	XX880C00-XX880DFC
Buffer 1	XX980400-XX9805FC	Buffer 1	XX980C00-XX980DFC
Buffer 2	XXA80400-XXA805FC	Buffer 2	XXA80C00-XXA80DFC
Buffer 3	XXB80400-XXB805FC	Buffer 3	XXB80C00-XXB80DFC

DataIO2 DAQ readout

Word count registers

Mezzanine card 1		Mezzanine card 2	
Channel 1		**Channel 1**	
Buffer 0	XX0C0800	Buffer 0	XX0C080C
Buffer 1	XX0C0900	Buffer 1	XX0C090C
Buffer 2	XX0C0A00	Buffer 2	XX0C0A0C
Buffer 3	XX0C0B00	Buffer 3	XX0C0B0C
Channel 2		**Channel 2**	
Buffer 0	XX0C0804	Buffer 0	XX0C0810
Buffer 1	XX0C0904	Buffer 1	XX0C0910
Buffer 2	XX0C0A04	Buffer 2	XX0C0A10
Buffer 3	XX0C0B04	Buffer 3	XX0C0B10
Channel 3		**Channel 3**	
Buffer 0	XX0C0808	Buffer 0	XX0C0814
Buffer 1	XX0C0908	Buffer 1	XX0C0914
Buffer 2	XX0C0A08	Buffer 2	XX0C0A14
Buffer 3	XX0C0B08	Buffer 3	XX0C0B14

RAM Read VME addresses

Mezzanine card 1		Mezzanine card 2	
Channel 1		**Channel 1**	
Buffer 0	XX8C0000-XX8C01FC	Buffer 0	XX8C0800-XX8C097C
Buffer 1	XX9C0000-XX9C01FC	Buffer 1	XX9C0800-XX9C097C
Buffer 2	XXAC0000-XXAC01FC	Buffer 2	XXAC0800-XXAC097C
Buffer 3	XXBC0000-XXBC01FC	Buffer 3	XXBC0800-XXBC097C
Channel 2		**Channel 2**	
Buffer 0	XX8C0200-XX8C3FC	Buffer 0	XX8C0A00-XX8C0BFC
Buffer 1	XX9C0200-XX9C03FC	Buffer 1	XX9C0A00-XX9C0BFC
Buffer 2	XXAC0200-XXAC03FC	Buffer 2	XXAC0A00-XXAC0BFC
Buffer 3	XXBC0200-XXBC03FC	Buffer 3	XXBC0A00-XXBC0BFC
Channel 3		**Channel 3**	
Buffer 0	XX8C0400-XX8C05FC	Buffer 0	XX8C0C00-XX8C0DFC
Buffer 1	XX9C0400-XX9C05FC	Buffer 1	XX9C0C00-XX9C0DFC
Buffer 2	XXAC0400-XXAC05FC	Buffer 2	XXAC0C00-XXAC0DFC
Buffer 3	XXBC0400-XXBC05FC	Buffer 3	XXBC0C00-XXBC0DFC

DAQ Readout

FPGA selection

VME address bits 18	19	Selected FPGA
0	0	Control FPGA
1	0	DataIO FPGA 1
1	1	DataIO FPGA 2

Registers

DataIO FPGA 1

Name	Address	Type
Firmware version	YY080000	R
Reset	YY080004	W
DAQ SW version	YY080008	R/W
Control register 1	YY08000C	R/W
Status register 1	YY080010	R
Pulse 1	YY080014	W
Control register 2	YY080018	R/W
Control register 3	YY08001C	R/W
Status register 2	YY080020	R

DataIO FPGA 2

Name	Address	Type
Firmware version	YY0C0000	R
Reset	YY0C0004	W
DAQ SW version	YY0C0008	R/W
Control register 1	YY0C000C	R/W
Status register 1	YY0C0010	R
Pulse 1	YY0C0014	W
Control register 2	YY0C0018	R/W
Control register 3	YY0C001C	R/W
Status register 2	YY0C0020	R

Control FPGA

Name	Address	Type
Firmware version	YY000000	R
Reset	YY000004	W
DAQ SW version	YY000008	R/W
Control register 1	YY00000C	R/W
Status register 1	YY000010	R
Pulse 1	YY000014	W
Control register 2	YY000018	R/W
Control register 3	YY00001C	R/W
Status register 2	YY000020	R

YY = VME address bits 31..24,
not used by the firmware.

FPGA selection

18	19	
0	0	Control FPGA
1	0	DataIO FPGA 1
1	1	DataIO FPGA 2

Table 1: VME address bits for FPGA selection

RAM selection

VME address bit 17	Selected DAQ RAM
0	DAQ RAM 1
1	DAQ RAM 2

Buffer selection

VME address bit 20	21	Selected buffer
0	0	Buffer 0
0	1	Buffer 1
1	0	Buffer 2
1	1	Buffer 3

Word count registers

DataIO FPGA 1

DAQ RAM	Buffer #	Address
1	0	YY080800
1	1	YY080900
1	2	YY080A00
1	3	YY080B00
2	0	YY080804
2	1	YY080904
2	2	YY080A04
2	3	YY080B04

DataIO FPGA 2

DAQ RAM	Buffer #	Address
1	0	YY0C0800
1	1	YY0C0900
1	2	YY0C0A00
1	3	YY0C0B00
2	0	YY0C0804
2	1	YY0C0904
2	2	YY0C0A04
2	3	YY0C0B04

Control FPGA

DAQ RAM	Buffer #	Address
1	0	YY000800
1	1	YY000900
1	2	YY000A00
1	3	YY000B00
2	0	YY000804
2	1	YY000904
2	2	YY000A04
2	3	YY000B04

YY = VME address bits 31..24, not used by the firmware.

DAQ Header word

Bit	Description
0..7	Bunch Counter Value
8..12	Geographical Address
13..22	Board Serial Number
23..31	Board Type

FIFO and DAQ RAM sizes

Muon

DataIO FPGA's

One Muon channel (eight / DataIO FPGA):

- Muon input FIFO: 512 x 8-bits
- Muon middle FIFO: 128 x 32-bits
- Muon output FIFO: 128 x 34-bits
- Muon input DAQ RAM: 128 x 32-bits

Control FPGA

Muon:

- Muon DataIO 1 input FIFO: 512 x 34-bits
- Muon DataIO 2 input FIFO: 512 x 34-bits

XTRP:

- XTRP input FIFO: 512 x 23-bits
- XTRP input DAQ RAM: 2048 x 32-bits

L1:

- L1 input FIFO: 16 x 64-bits

Output:

- Output FIFO: 1024 x 32-bits
- Output DAQ RAM: 2048 x 32-bits

CLUSTER

DataIO FPGA

ISOLIST:

- Input FIFO: 512 x 8-bits
- ISOPICK FIFO: 8 x 88-bits x 6
- ISOCLIQUE FIFO: 8 x 16-bits
- Output FIFO: 1024 x 32-bits
- Input DAQ RAM: 256 x 32-bits
- Output DAQ RAM: ???

CLIST:

- Input FIFO: 512 x 8-bits
- CLIST FIFO 128 x 50-bits
- Input DAQ RAM: 256 x 32-bits
- Output FIFO: 1024 x 32-bits
- Output DAQ RAM: ???

Control FPGA

- L1 Input FIFO: 16 x 32-bits
- DataIO 1 Input FIFO: 512 x 32-bits
- DataIO 2 Input FIFO: 512 x 32-bits
- Output FIFO 2048 x 32-bits
- Output DAQ RAM: 2048 x 32-bits

ShowerMax

DataIO FPGA's

One ShowerMax channel (eight / DataIO FPGA):

- Input FIFO: 128 x 8-bits
- Middle FIFO: 32 x 32-bits
- Output FIFO: 32 x 32-bits
- Input DAQ RAM: 8 x 32-bits

Control FPGA

- Output FIFO: 2048 x 32-bits
- Output DAQ RAM: 2048 x 32-bits

SVT

Control FPGA

Input:

- Middle FIFO: 512 x 23-bits
- Input DAQ RAM: 2048 x 32-bits

Output:

- Output FIFO: 2048 x 32-bits
- Output DAQ RAM: 2048 x 32-bits

XFT

DataIO FPGA's

One XFT channel (six / DataIO FPGA):

- Input FIFO: 32 x 16-bits
- Output FIFO:
    - First channel: 256 x 32-bits
    - Other channels: 512 x 32-bits
- Onput DAQ RAM: 512 x 32-bits

Control FPGA

- Output FIFO: 2048 x 32-bits
- Output DAQ RAM: 2048 x 32-bits

S-LINK

DataIO FPGA's

One S-LINK channel (two / DataIO FPGA):

- Input FIFO: 256 x 32-bits
- Output FIFO: 512 x 32-bits
- Input DAQ RAM: 2048 x 32-bits

Control FPGA

- DataIO FPGA 1 input FIFO: 512 x 32-bits
- DataIO FPGA 2 input FIFO: 512 x 32-bits
- Output FIFO: 2048 x 32-bits
- Output DAQ RAM: 2048 x 32-bits

L2toTS

RAM and FIFO sizes

DataIO FPGA

- Input FIFO: 512 x 32-bits
- Input DAQ RAM: 4096 x 32-bits
- Latency DAQ RAM: 2 x 32-bits

Control FPGA

- Input FIFO: 16 x 32-bits
- Latency DAQ RAM: 3 x 32-bits