Introduction to FPGA Design

Physics 536 – Spring 2009

Illustrating the FPGA design process using Quartus II design software and the Cyclone II FPGA Starter Board.

Why FPGA's?

- Digital logic:
 - Equivalent to a large number of discrete logic elements
 - NOT a microprocessor (although microprocessors can be implemented in an FPGA design)
- High density:
 - All the logic is inside a single chip
 - No need for interconnecting traces on PCB between logic circuits
- Reprogrammable:
 - Designs can be changed after the hardware has been manufactured
 - High-level design software optimizes the usage of limited resources

FPGA Resources

- Both companies produce competitive products neither is endorsed. Other companies exist...
- We use Altera tools to demonstrate the design process.
- Xilinx has a similar set of tools.
- Conceptually, the design process is the same.

Cyclone II FPGA Starter Board



Example Design Problem

- Implement a 4-input XOR function:
 - Output will be high only when exactly one input is high.
 - Use KEY[0..3] as inputs.
 - Show output on green LED.
- Boolean algebra:

$$Q = D_0 \cdot \bar{D}_1 \cdot \bar{D}_2 \cdot \bar{D}_3 + \bar{D}_0 \cdot D_1 \cdot \bar{D}_2 \cdot \bar{D}_3 + \bar{D}_0 \cdot \bar{D}_1 \cdot D_2 \cdot \bar{D}_3 + \bar{D}_0 \cdot \bar{D}_1 \cdot \bar{D}_2 \cdot D_3$$

• We could simplify this, but choose not to.

Design Flow



- Design entry:
 - Schematic entry
 - High level language
- Synthesis:
 - Translating design into logic elements
- Simulation:
 - Validate design logic
- Fitting:
 - Implementing logic using FPGA resources

Altera FPGA Design Software



Please be patient...

Altera software is installed under C:\Altera\...

This might happen...



Altera Licensing Information



Ready to begin:



Starting a New Project

- File → New Project Wizard...
- "What is the working directory for this project?"
 H:\Physics536
- "What is the name of this project?"
 - FirstExample
- "What is the name of the top-level entity...?"
 - FirstExample (default)
- Then click "Next >"... Click "Yes" to create the directory.
- No need to add design files, so click "Next >".

Starting a New Project

- Select the device:
 - Family: Cyclone II
 - Device: EP2C20F484C7
- Then click "Finish".

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EP2C20F484C7	1.2V	18752	315	239616	52	4	
EP2C20F484C8	1.2V	18752	315	239616	52	4	
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A Really, Really Simple Design

- If you can't get something simple to work, don't expect to be able to do anything complicated...
- A much simpler design:
 - Input KEY0
 - Output to green LEDG0



Entering the Simple Design

File → New → "Block Diagram/Schematic File"



Adding the Inputs/Outputs

- Click on ____
 - navigate to .../primitives/pin/input
 - Click OK, click to place the pin.
- Do the same for the output pin.

Symbol		X
Libraries: C:/altera/72/quartus/libraries/ C:/altera/72/quartus/libraries/ C:/altera/72/quartus/libraries/ C:/altera/72/quartus/libraries/ C:/altera/72/quartus/libraries/		· · · · · · · · · · · · · · · · · · ·
⊕ buffer ⊕ buffer ⊕ other ⊕ pin ↓ ⊕ ↓ ⊕ ↓ ↓		· · · · · ·
Name:	pin_name WPUT	
 Repeat-insert mode Insert symbol as block Launch MegaWizard Plug-in 		· · · · · · · · · · · · · · · · · · ·
MegaWizard Plug-In Manager		

Adding a Buffer

 Buffers can be used to drive special signals in the FPGA. In this case we don't need anything special so we can select

.../primitives/buffer/wire

 Click the "Wire" tool () and connect the pins to the buffer.

Labeling the Pins Double-click on the text associated with the pins



Compiling the Design

• File \rightarrow Save Project

Total pins:

- Processing → Start Compilation
- Success? If not, fix the problem; try again.
- Look at resource usage:

Total logic elements: 0/18,752 (0%) 2/315 (<1%)

Not too surprising...

 But wait... how does it know which pins are physically wired to KEY[0] and LEDG[0]?

Assigning Pins

- Pins can be assigned individually:
 - Assignments \rightarrow Pins
- Or imported from a file:
 - Assignments → Import Assignments

Import Assignments	
Specify the source and categories of assignments to import. Click LogicLock Import File Assignments to select LogicLock Import File(s). To Assignment source	I
File name: C:/Altera/Kits/Cyclonell_Starter_Kit-v1.0.0/Examples/CII_Starter_demonstrations/design_files/CII_Starter_pin_assignments.csv	Categories
C Use LogicLock Import File Assignments	Advanced
LogicLock Import File Assignments	
Copy existing assignments into FirstExample.qsf.bak before importing	Cancel

C:\Altera\Kits\CycloneII_Starter_Kit-v1.0.0/...

.../Examples/CII_Starter_demonstrations/design_files/CII_Starter_pin_assignments.csv

• Don't forget to re-compile the design.

Downloading the Design

- Plug in and turn on the DC power
- Plug in the USB cable.
- Tools \rightarrow Programmer \rightarrow Start



Did It Work?

• Sort of...



4-Input XOR

- Invert the KEY[0..3] inputs before assigning them to D₀, D₁, D₂, D₃.
- Use .../primitives/logic/not for inverter
- Implement the logic:

$$Q = D_0 \cdot \bar{D}_1 \cdot \bar{D}_2 \cdot \bar{D}_3 + \bar{D}_0 \cdot D_1 \cdot \bar{D}_2 \cdot \bar{D}_3 + \bar{D}_0 \cdot \bar{D}_1 \cdot D_2 \cdot \bar{D}_3 + \bar{D}_0 \cdot \bar{D}_1 \cdot \bar{D}_2 \cdot D_3$$

- Use 4-input AND and 4-input OR gates:
 - .../primitives/logic/and4
 - .../primitives/logic/or4

More complicated schematic

Can you spot the mistake? The compiler certainly can!



Simulate the Design

- We need to specify all possible inputs.
- File → New... → Other Files →
 Waveform Vector File

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Specifying Input Values

 Right-click under "Name" → Insert → Insert Node or Bus…

lame:	KEY[03]		OK
Гуре:	INPUT	•	Cancel
Value type:	9-Level	-	Node Finder
Radix:	Hexadecimal	•	
Bus width:	4		
Start index:	0		

Specifying Input Values

- Left-click on the "KEY" signal.

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File → Save...

H:\Physics536\FirstExample\Waveform1.wvf

Configure the Simulator

- Processing \rightarrow Simulator Tool
- Simulation input: H:\Physics536\FirstExample\Waveform1.wvf

Simulator Tool			
Simulation mode: Timing		Generate Fund	tional simulation inedist
Simulation input: Waveform1.vwf			Add Multiple Files
Simulation period			
Run simulation until all vector si	stimuli are used		
C End simulation at: 100	ns 💌		
- Simulation options			
Automatically add pins to simula	lation output wavefor	ns	
Check outputs Waveform	Comparison Settings.		
Setup and hold time violation d	detection		
Glitch detection: 1.0	ns 💌		
Overwrite simulation input file w	with simulation results		
Generate Signal Activity File:			
Generate VCD File:			
	0 % 00:00:00		
🚬 Start 👘 Stop	p 🖣	Dpen	Report

• Click "Start", then "Open" to examine the output.

Examine the Output

• Does this look right?



- We should expect only 1110, 1101, 1011 and 0111 to give and output of 1...
- Check the timing report...

Results of Timing Analysis

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ii I	Ū,	Info: ************************************	
. E	۰ (۱)	Info: Running Quartus II Classic Timing Analyzer	
	۰ (۱)	Info: Command: quartus_tanread_settings_files=offwrite_settings_files=off FirstExample -c FirstExampletiming_analysis_only	
Đ	۰ (۱)	Info: Longest tpd from source pin "KEY[1]" to destination pin "LEDG[0]" is 10.246 ns	
(E	۰ (۱)	Info: Quartus II Classic Timing Analyzer was successful. O errors, O warnings	
	۰.	Info: Quartus II Full Compilation was successful. O errors, 441 warnings	
			~
₿ \ Sj	ystem (69)	A Processing (50) Λ Extra Info λ Info (44) λ Warning (6) λ Critical Warning λ Error λ Suppressed (6) λ Flag /	

- Longest tpd (propagation delay) from source pin "KEY[1]" to destination pin "LEDG[0]" is 10.24 ns.
- Increase period of each input vector from 10ns to 50 ns...

Simulation Analysis

Master Time Bar: 15.55 ns				·I·I	Pointer: 1/				07.04 ns			Interval:			91.49 ns			S	Start:			End:									
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- Now this looks like what one would expect.
- Try downloading the FPGA with this configuration and try it out.

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