PURDUE UNIVERSITY DEPARTMENT OF PHYSICS

Physics 53600

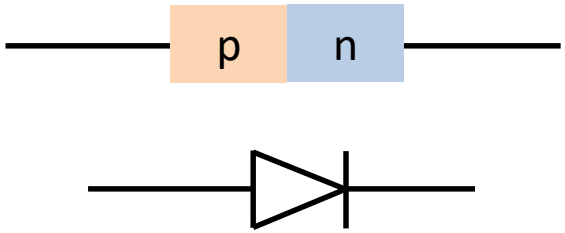
Electronics Techniques for Research

Now in PowerPoint!

Spring 2020 Semester

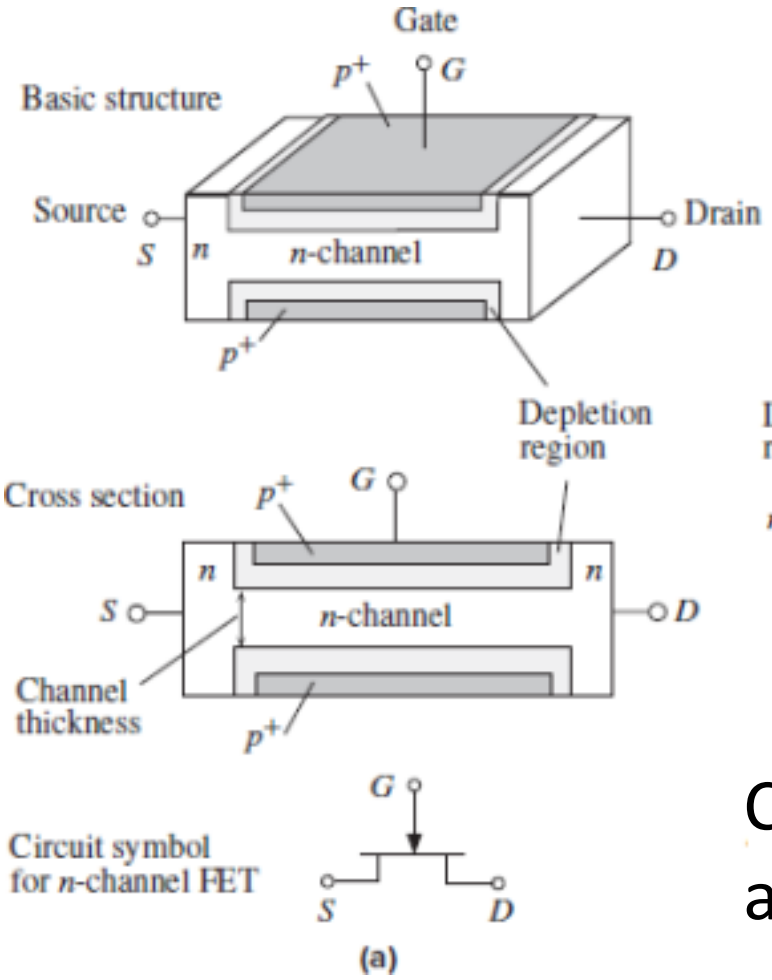
Prof. Matthew Jones

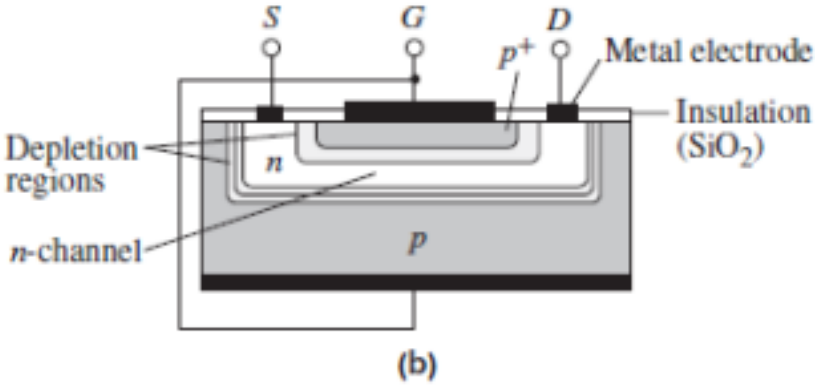
PN Junction Diodes



- If $V_n < V_p$ then the width of the depletion region shrinks, there are lots of charge carriers available, and current flows.
- If $V_n > V_p$ then the width of the depletion region increases and the diode is reverse biased (no current flows)

Junction Field Effect Transistors

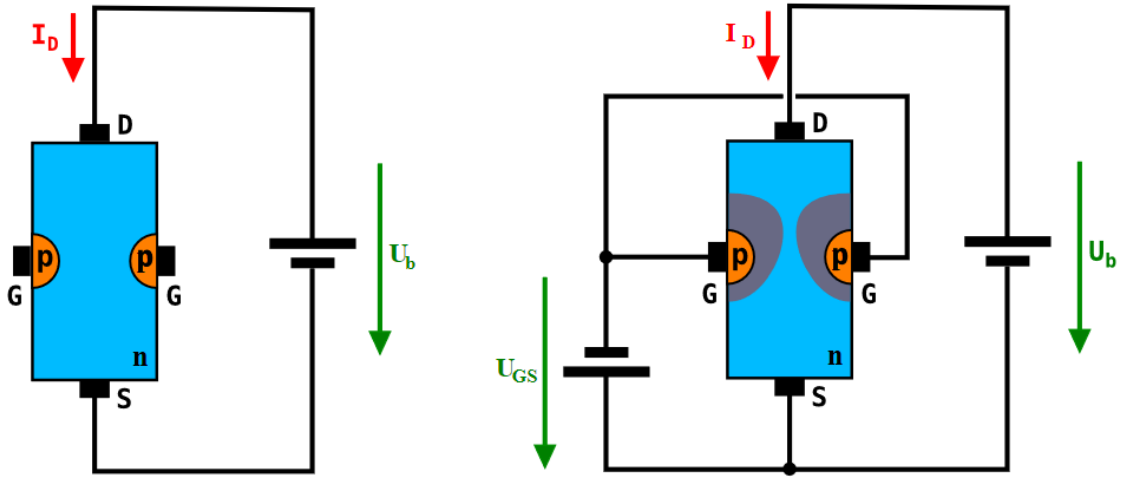




Current flows *into* the drain and flows *out of* the source.

Junction Field Effect Transistors

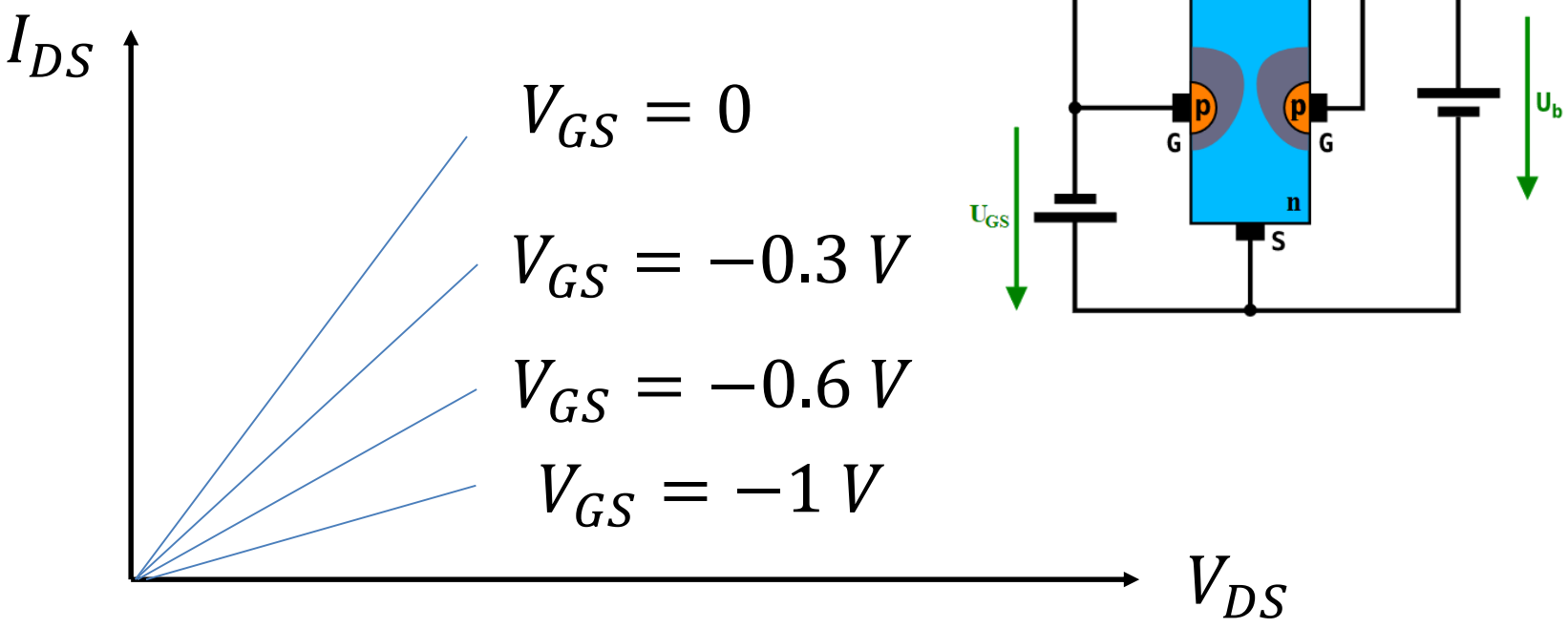
- Initially, the depletion regions around the gate are relatively small and a conducting channel remains between the source and the drain
- Applying a negative voltage to the gate increases the depth of the depletion region



$V_n > V_p$

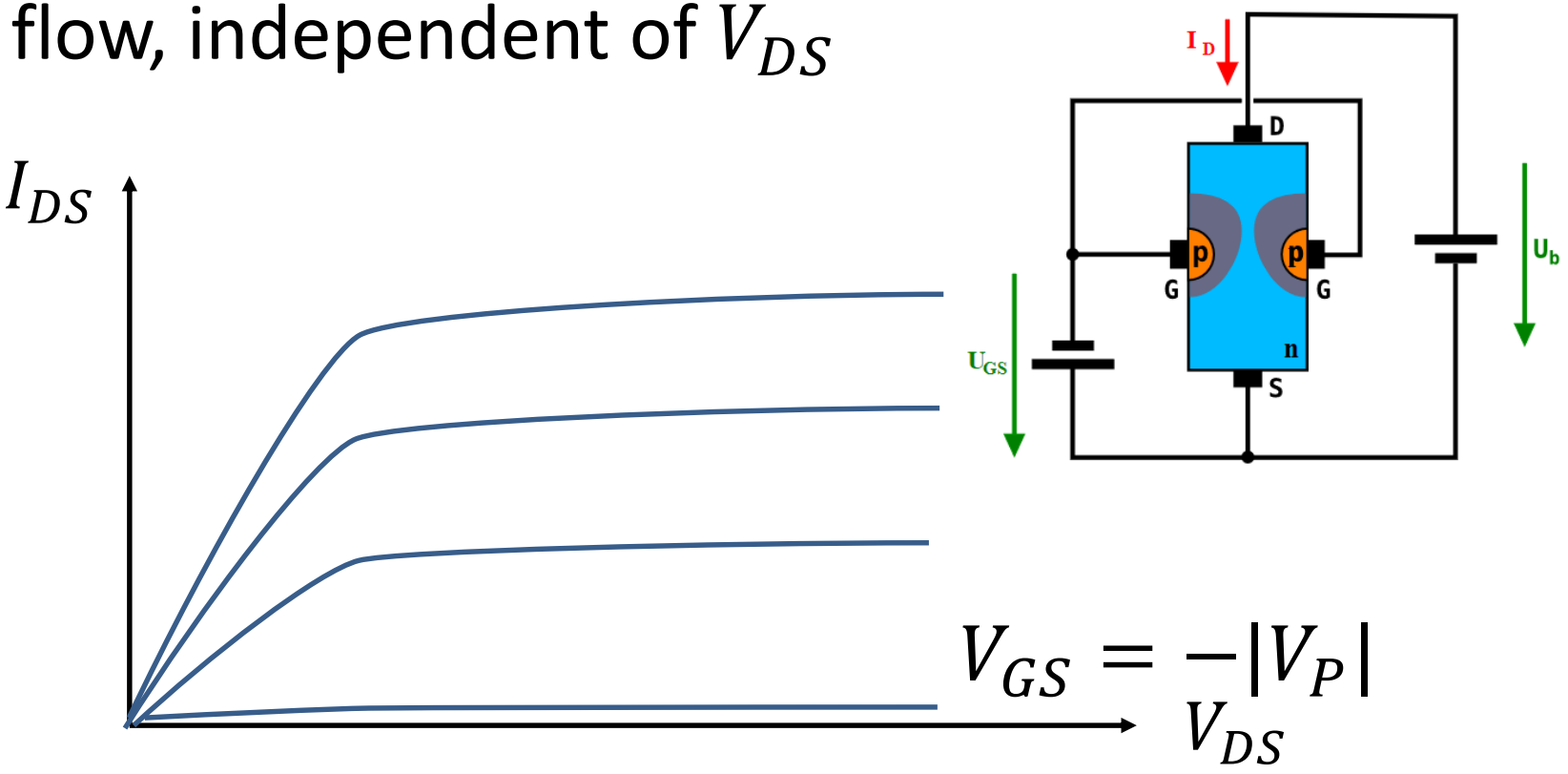
Junction Field Effect Transistors

- For small V_{DS}, the n-channel behaves like a voltage controlled resistor



Junction Field Effect Transistors

- Charge carriers in the n-channel are limited, so there is a maximum possible current that can flow, independent of V_{DS}



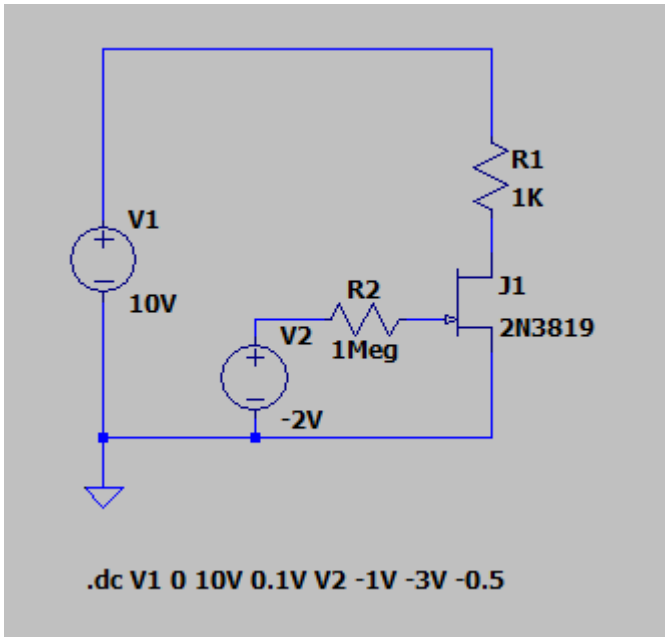
Junction Field Effect Transistors

- When $V_{GS} = -|V_P|$, the channel is "pinched off" and no current can flow
- In the active region (current source) the current is given by:

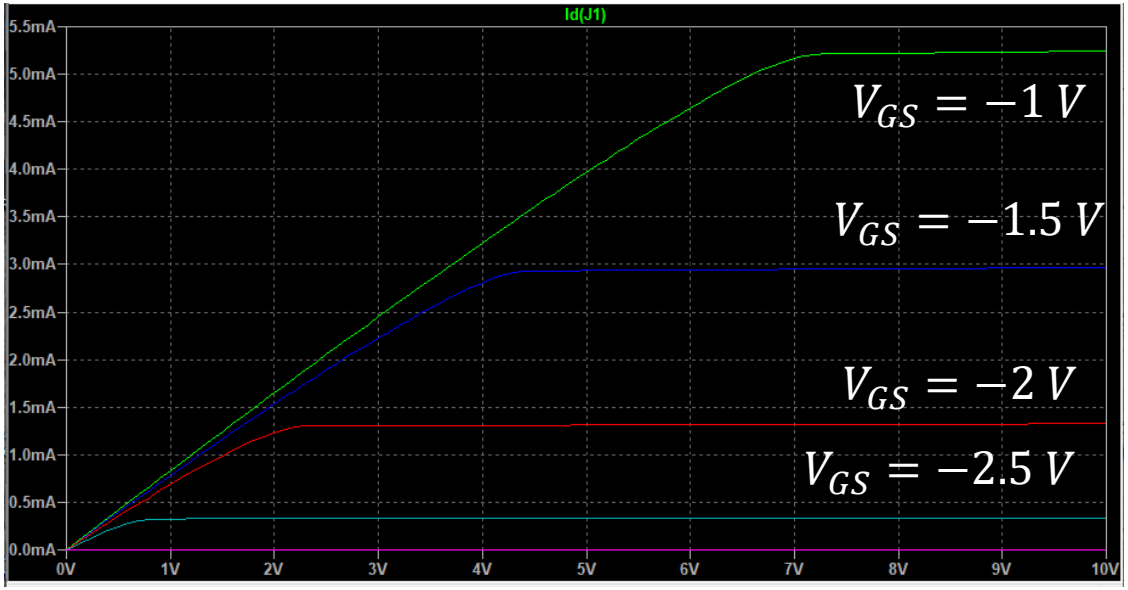
$$I_D = I_{DSS}\left(1 + \frac{V_{GS}}{|V_P|}\right)^2$$

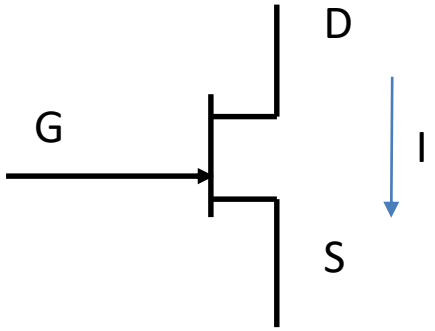
- Recall that $V_{GS} < 0$, so $I_D = 0$ when $V_{GS} = -|V_P|$
- This forms a voltage-controlled current source
- Typical values: $I_{DSS} = 10\ \text{mA}, |V_P| = 3\ \text{V}$

JFET Circuits



2N3819 is a depletion mode n-channel JFET





JFET Circuits

2N3819

JFET VHF/UHF Amplifier

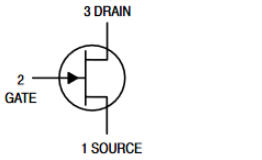
N–Channel – Depletion

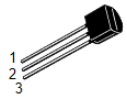
ON Semiconductor®

http://onsemi.com

MAXIMUM RATINGS

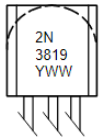
Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	25	Vdc
Gate–Source Voltage	V_{GS}	25	Vdc
Drain Current	I_D	100	mAdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	 350 2.8	 mW mW/°C
Storage Channel Temperature Range	T_{stg}	–65 to +150	°C





TO–92
CASE 29
STYLE 22

MARKING DIAGRAM



2N3819 = Device Code
Y = Year
WW = Work Week

Small Signal Gain

- A small change in voltage at the gate will change the current:

$$I_D = I_{DSS}\left(1 + \frac{V_{GS}}{|V_P|}\right)^2$$

$$\delta I_D = 2I_{DSS}\left(1 + \frac{V_{GS}}{|V_P|}\right)\frac{\delta V_{GS}}{|V_P|}$$

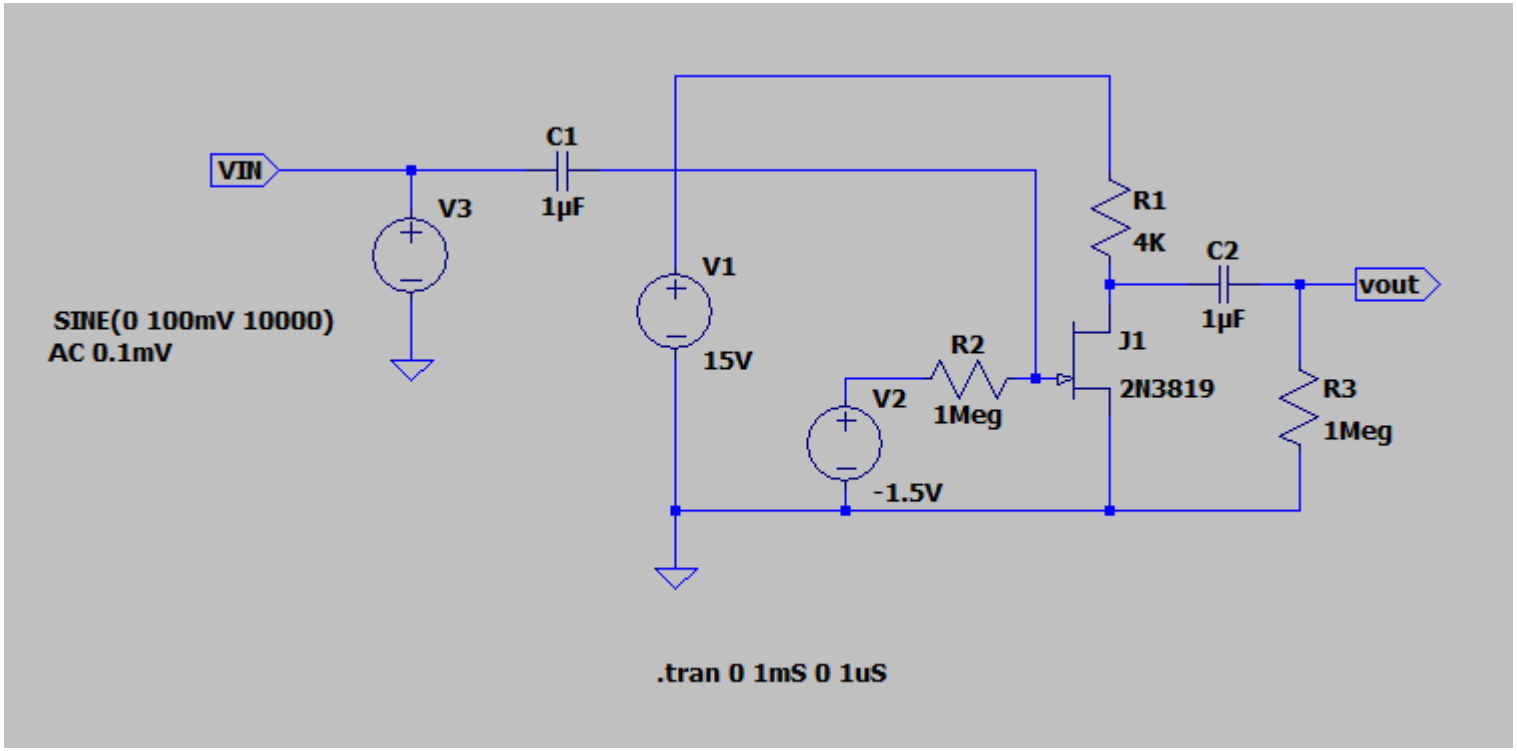
- Change in voltage at the source:

$$\delta V_S = -R\ \delta I_D$$

- Voltage gain:

$$A = \frac{\delta V_S}{\delta V_{GS}} = -2R\ \frac{I_{DSS}}{|V_P|}\left(1 + \frac{V_{GS}}{|V_P|}\right)$$

JFET Amplifier



Input impedance: $R2 = 1\ \mathrm{M}\Omega$

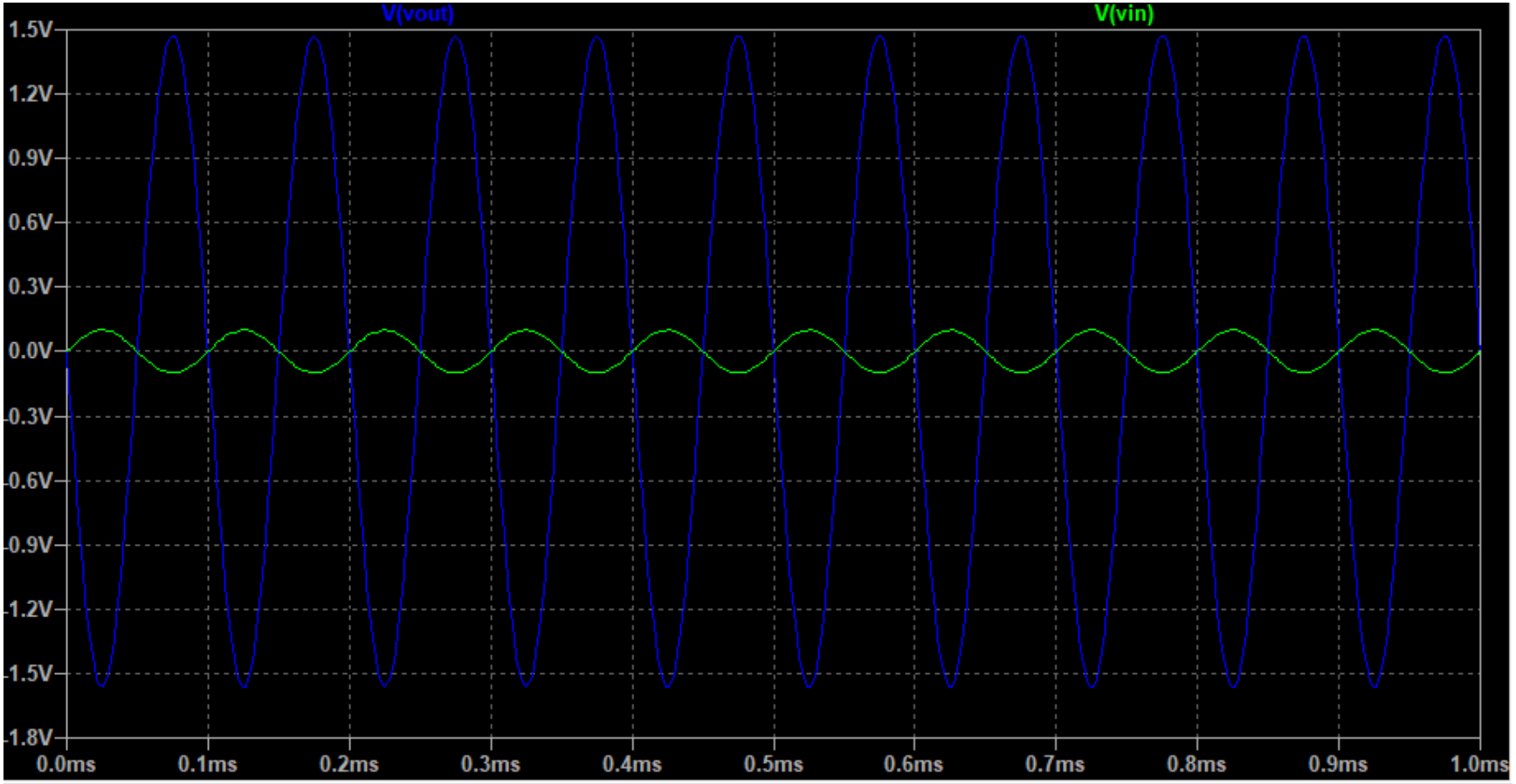
Output impedance: $R1 = 4\ k\Omega$

$$A = -2 \cdot (4\ k\Omega) \cdot \left(\frac{11.7\ mA}{3\ V}\right) \cdot \frac{1}{2}$$

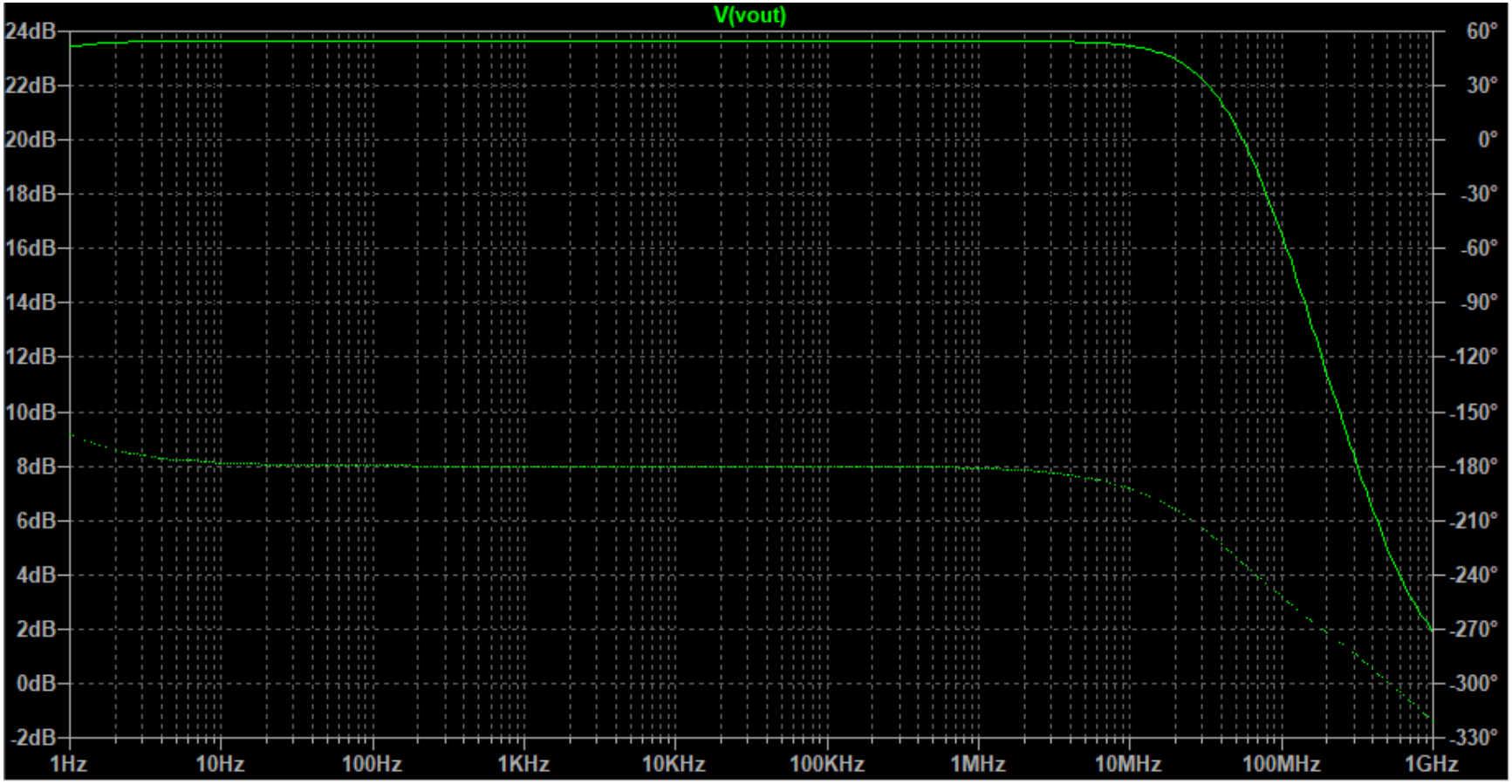
$$= -15.6$$

$$G = 24\ dB$$

JFET Amplifier

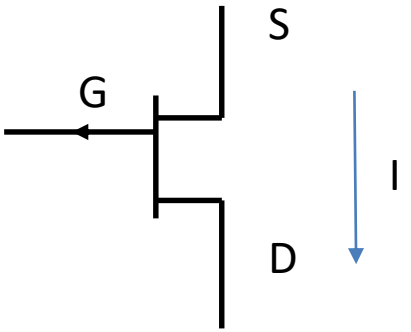


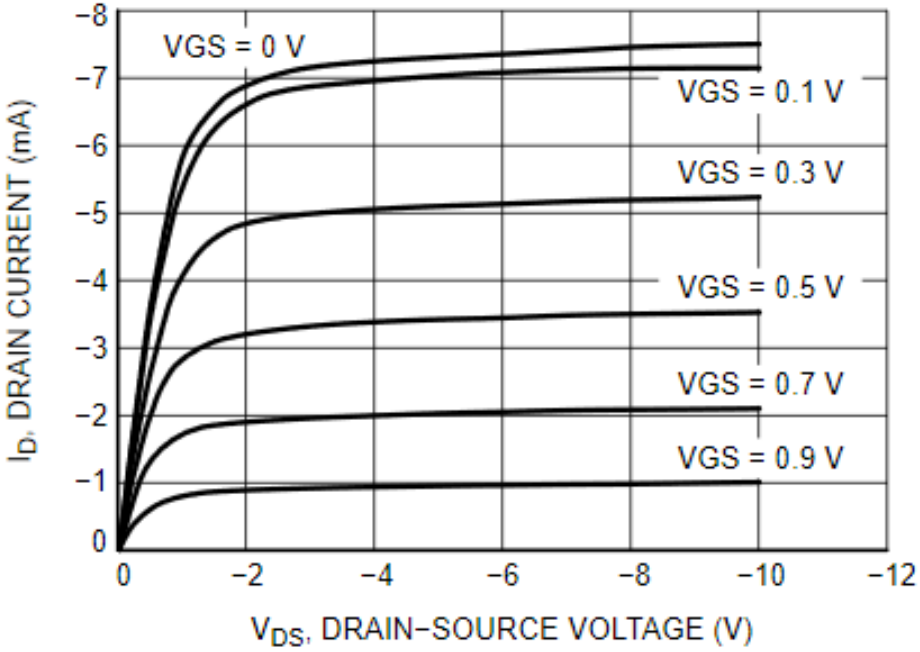
JFET Amplifier



P-channel JFET

- A P-channel JFET is reverse biased when $V_n > V_p$ but since now the gate is a n-type material, the current is restricted when $V_{GS} > 0$.
- Now the drain must be more negative than the source





Planar Semiconductor Manufacturing

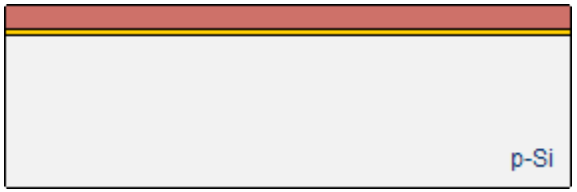
- The fabrication of semiconductors using photolithographic processes on planar substrates revolutionized the electronics industry.
- Consider the following process…
  https://www.halbleiter.org/en/fundamentals/construction-of-a-field-effect-transistor/

Planar Semiconductor Manufacturing

1. Start with a P-doped silicon substrate:

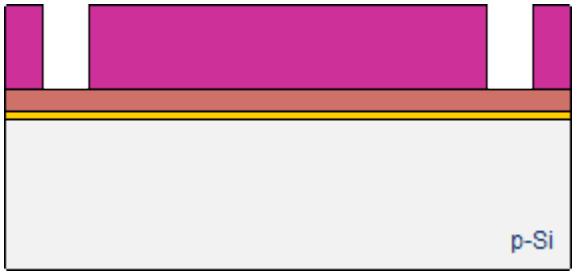
2. Oxidation creates a thin insulating layer of SiO_2:

3. A nitride layer is deposited on top:

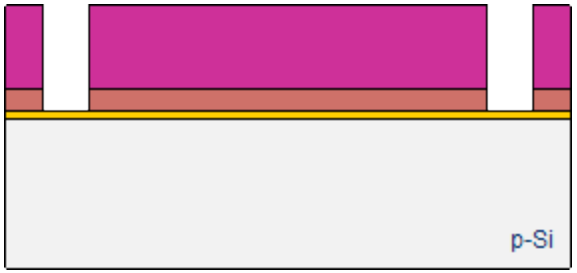


Planar Semiconductor Manufacturing

4. Apply a photoresist, expose and develop:

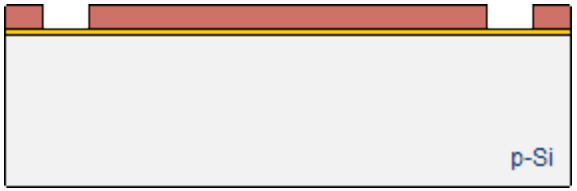


5. Etch through the nitride layer

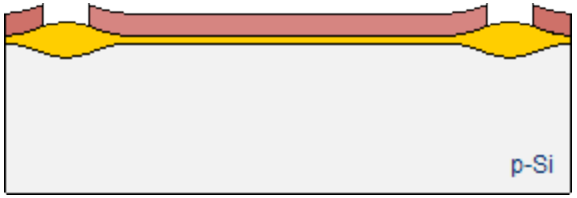


Planar Semiconductor Manufacturing

6. Remove photoresist



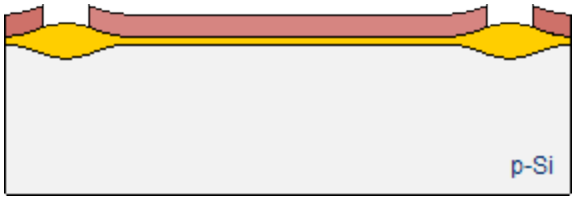
7. Grow additional oxide in the exposed regions to provide lateral isolation



Planar Semiconductor Manufacturing

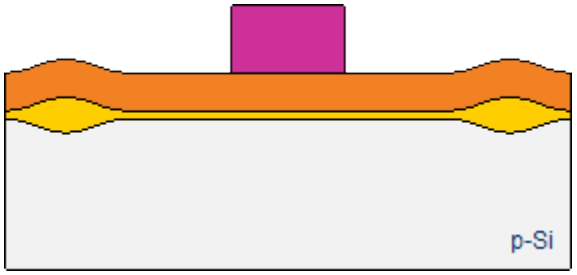
8. Etch nitride layer

9. Deposit polycrystalline silicon:

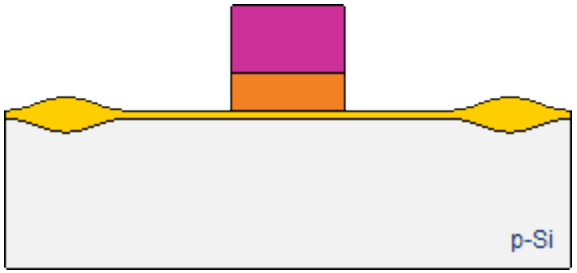


Planar Semiconductor Manufacturing

10. More photolithography



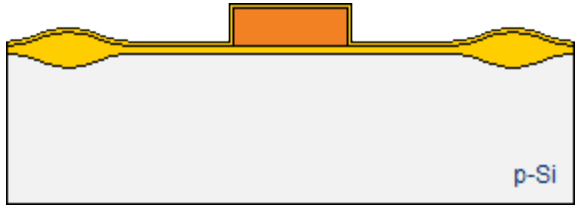
11. Etch the polycrystalline silicon



Planar Semiconductor Manufacturing

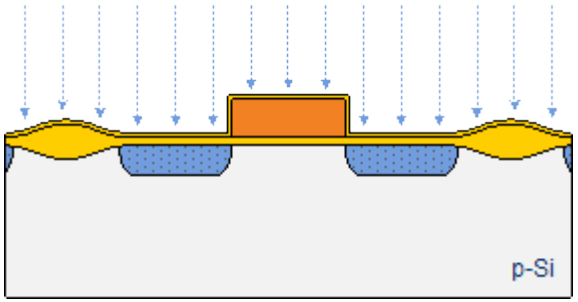
12. Remove photoresist

13. Apply a thin oxide layer over everything:

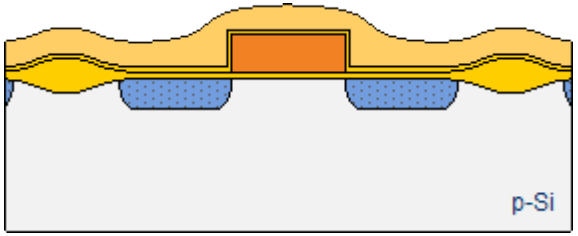


Planar Semiconductor Manufacturing

14. Phosphorus ion implantation:

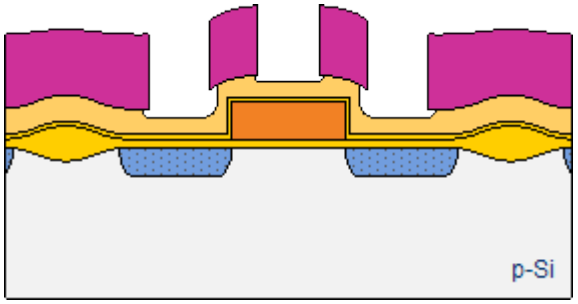


15. Apply a conformal insulating layer of oxide:

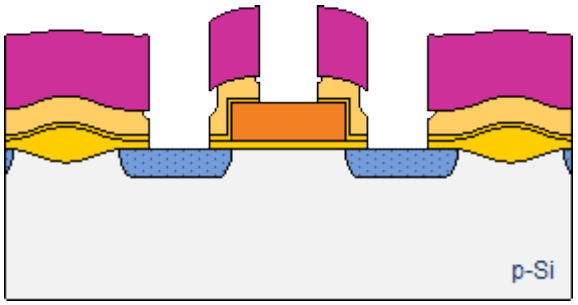


Planar Semiconductor Manufacturing

16. More photolithography:

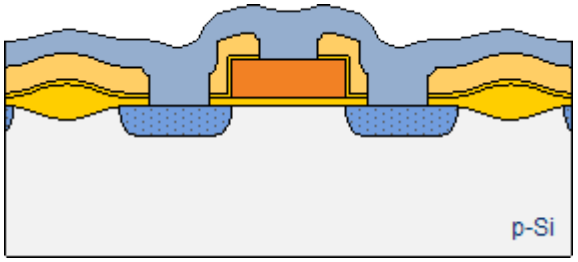


17. Etch the oxide layers:

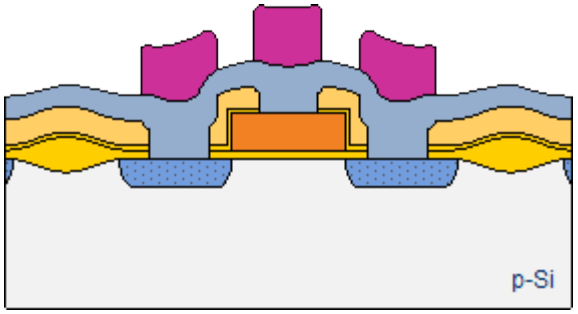


Planar Semiconductor Manufacturing

18. Remove photoresist and deposit metal:

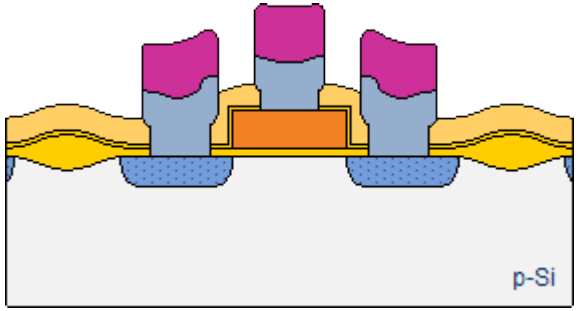


19. Even more photolithography:

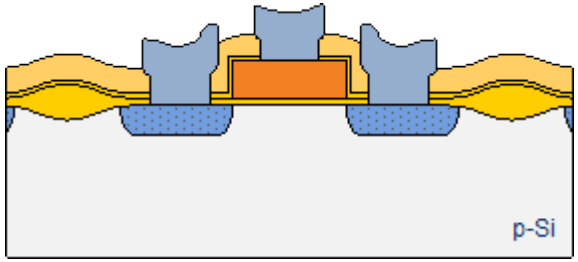


Planar Semiconductor Manufacturing

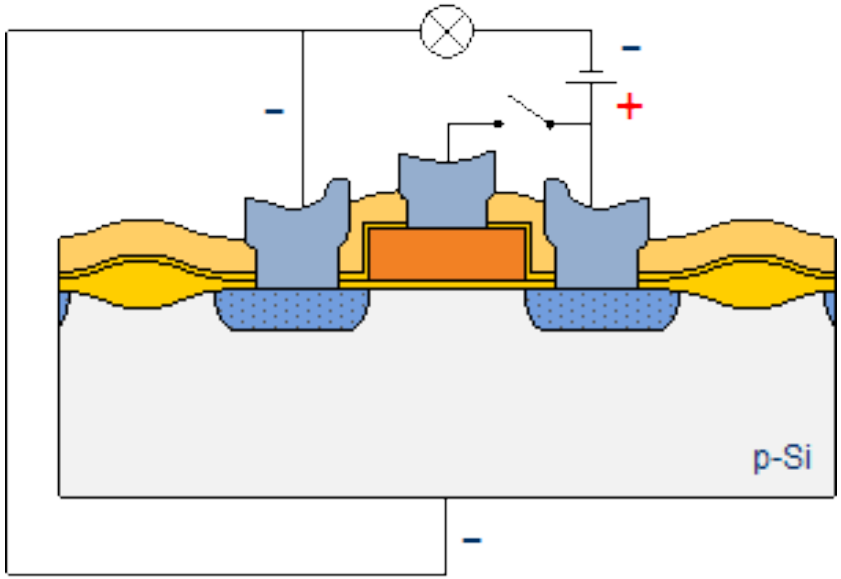
20. Etch the metal layer:



21. Remove photoresist:

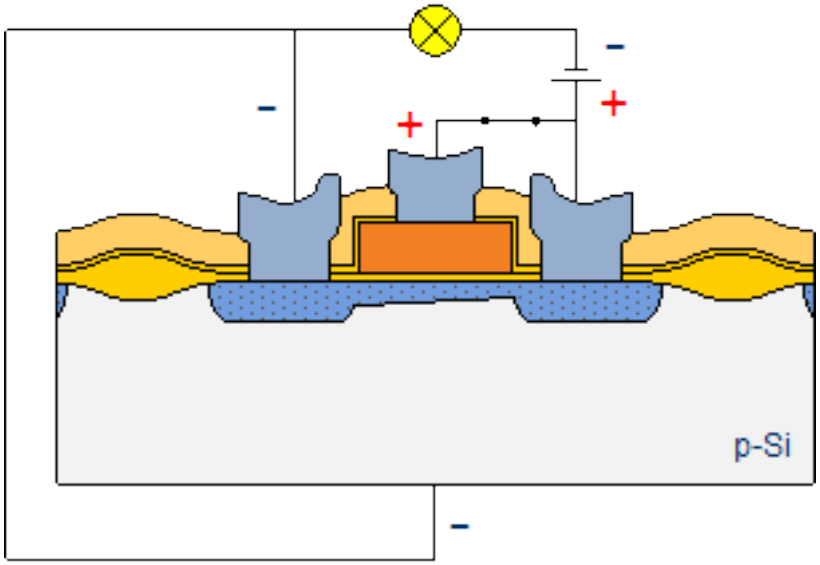


N-Channel Field Effect Transistor



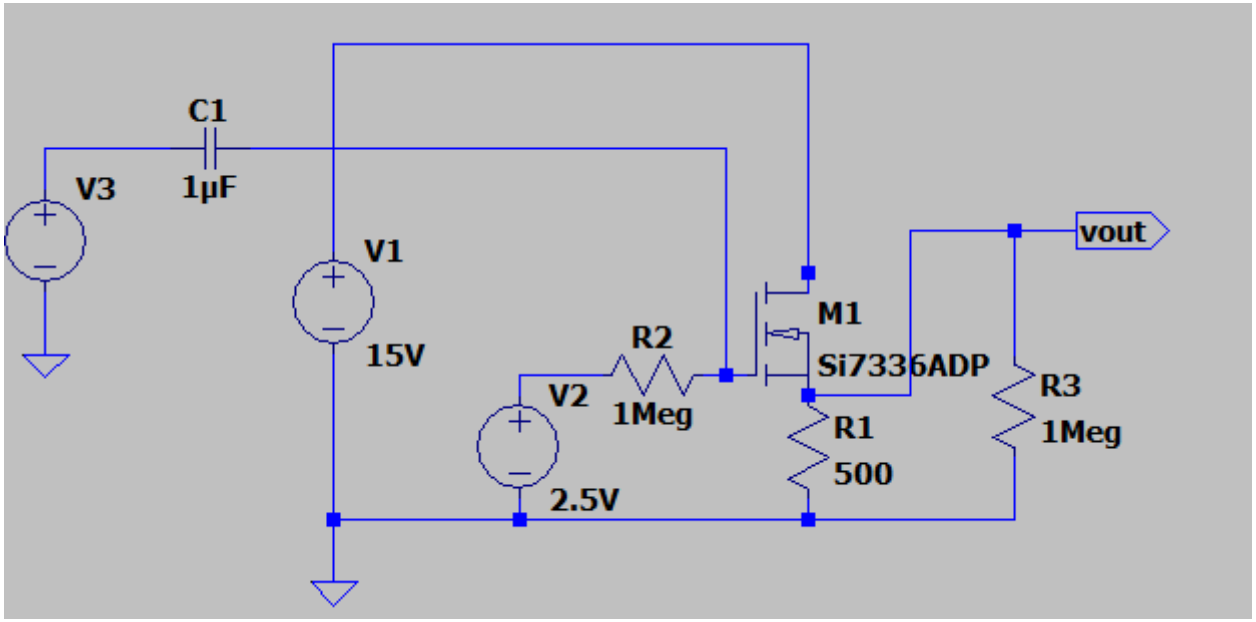
- No charge carriers are present in the channel between the n-type implants.
- No current can flow through the channel.

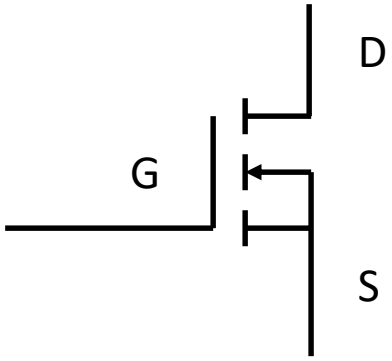
N-Channel Field Effect Transistor



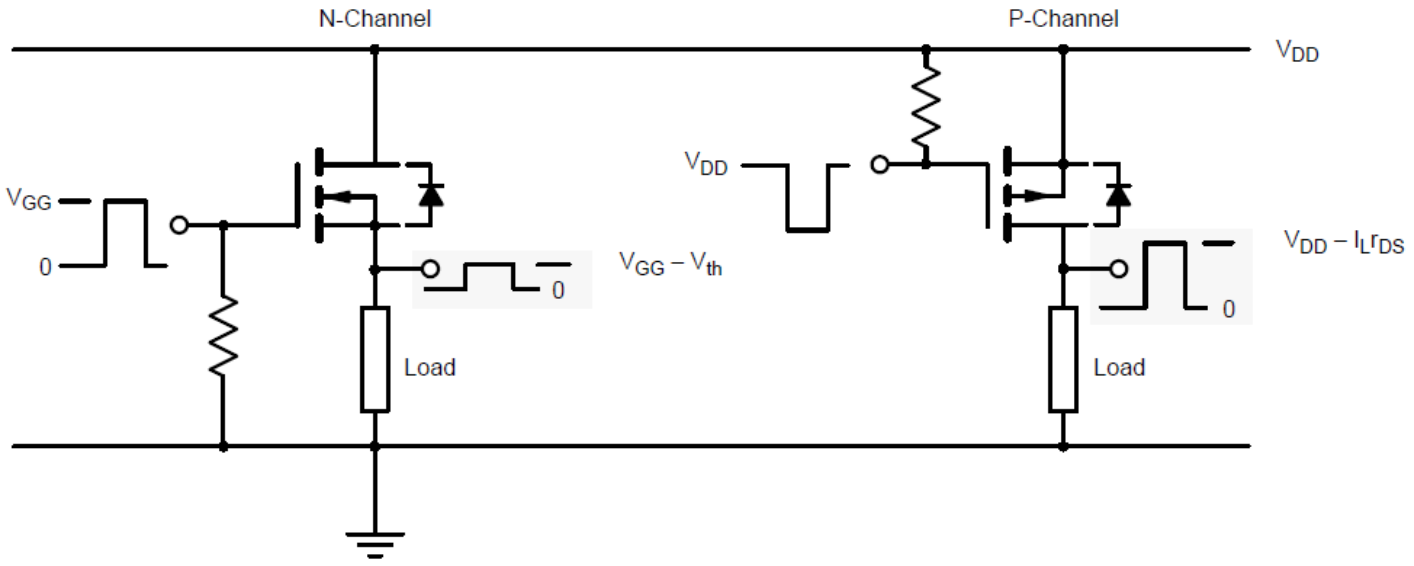
- A positive voltage applied to the gate attracts electrons from the substrate into the channel (enhancement).
- Now there are charge carriers and current can flow.
- The current is limited by the availability of charge carriers.

MOSFETs

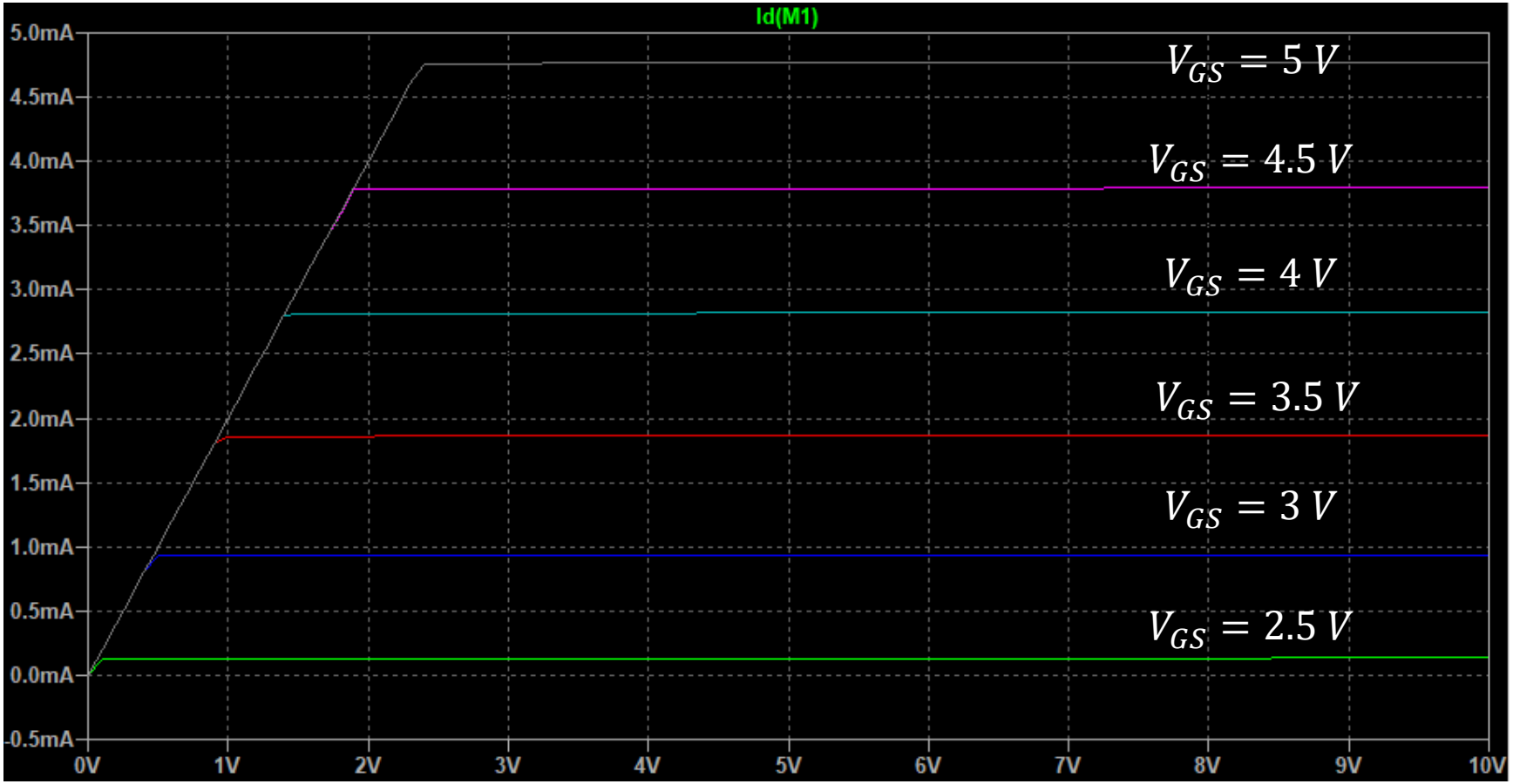

C1
1µF
V3
V1
15V
V2
2.5V
R2
1Meg
M1
Si7336ADP
R1
500
R3
1Meg
vout


D
G
S

MOSFETs


N-Channel
P-Channel
V_{DD}
V_{GG}
0
$V_{GG} - V_{th}$
0
Load
V_{DD}
$V_{DD} - I_L r_{DS}$
0
Load
(1a)
(1b)

MOSFETs


Id(M1)
5.0mA
4.5mA
4.0mA
3.5mA
3.0mA
2.5mA
2.0mA
1.5mA
1.0mA
0.5mA
0.0mA
-0.5mA
0V
1V
2V
3V
4V
5V
6V
7V
8V
9V
10V
$V_{GS} = 5\ V$
$V_{GS} = 4.5\ V$
$V_{GS} = 4\ V$
$V_{GS} = 3.5\ V$
$V_{GS} = 3\ V$
$V_{GS} = 2.5\ V$