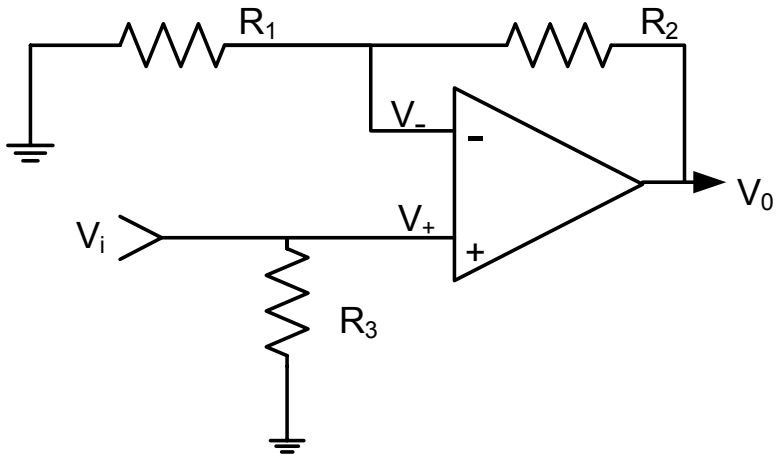
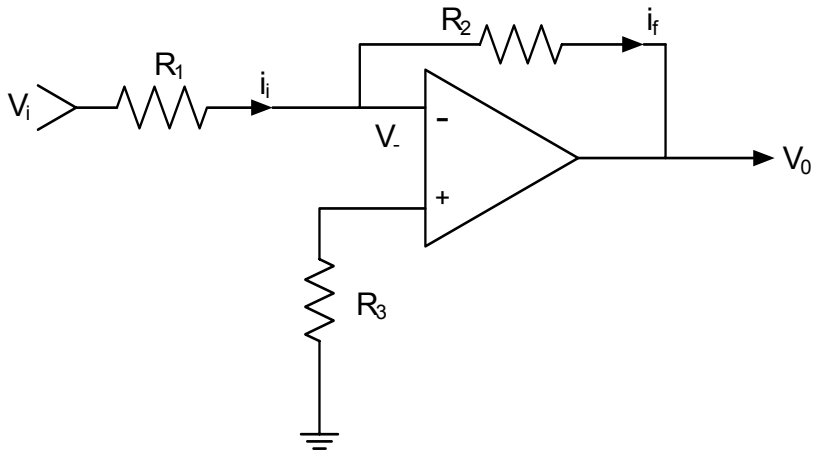
PHYSICS 536
Applications of the Golden Rules for Negative Feedback

The purpose of this experiment is to illustrate the "golden rules" of negative feedback for a variety of circuits. These concepts permit you to create and understand a vast number of practical circuits using only two simple rules. The op-amps used in this experiment are fully compensated, *i.e.* the open-loop phase shift is less than 135° to reduce the danger of oscillation. However, for future applications you should remember that a compensated op-amp can oscillate if additional phase shift is introduced accidentally in the feedback loop.



Op-amp Rule I. In the frequency range where the open loop gain of the op-amp, A, is much greater than the gain with feedback, i.e. A >> G_O, the voltage at the inverting input will be equal to the voltage at the non-inverting input. That is to say, the inputs of the op-amp become a virtual ground, $V_- = V_+$.

Op-amp Rule II. In the frequency range where A >> G_O, the feedback current will be equal to the input signal current. That is to say, $i_f \cong i_i$. This means that the op-amp effectively draws no current.



The maximum output signal voltage (peak-to-peak) is limited by the slew rate

$$V_{pp} \le \frac{\Delta V / \Delta t (V/\mu s)}{\pi f\,(MHz)} \qquad (12.1)$$

The slew rate is in volts / μ sec and the frequency I in MHz. The gain of a non-inverting amplifier is

$$G = \frac{G_O}{1 + jf / f_{bc}} = \frac{R_1 + R2}{R_1} \frac{1}{1 + jf / f_{bc}} \tag{12.2}$$

where the break frequency is $f_{bc} = f_T / G_O$. The rate of voltage change caused by current (I) flowing into a capacitor is

$$\frac{\Delta V}{\Delta \mathrm{T}} = \frac{\mathrm{I}}{C} \tag{12.3}$$

The gate to source voltage of a FET is

$$V_{gs} = V_T \left(1 - \sqrt{I_d / I_{dss}}\right) \tag{12.4}$$

A. Op-Amp Comparison at Higher Frequency.

In this section you will compare the performance of a general purpose 741 op-amp to a relatively high speed LM318 op-amp in the non-inverting amplifier circuit shown below. Always use by-pass capacitors (refer to GIL section 13.2), and turn off the power supplies before components are changed.

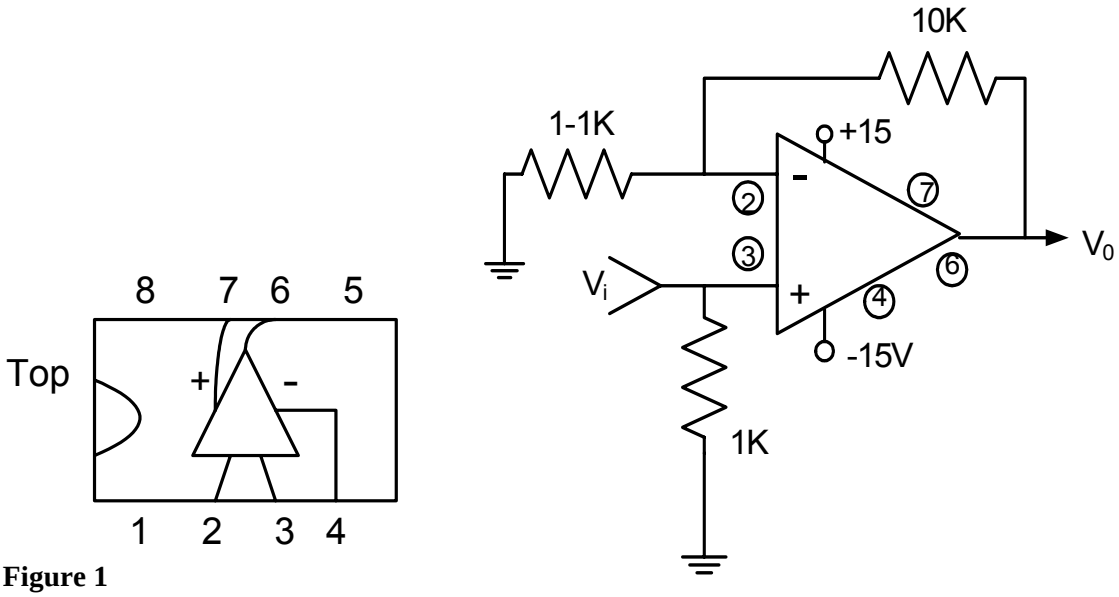


Figure 1

1. Calculate the midfrequency closed-loop gain. For both op-amps, calculate the closed loop break frequency and the maximum amplitude signal that can be obtained at f_{bc} without slew rate distortion. Use the following typical specifications for these op-amps. Include these calculations in your laboratory report.

Op-Amp	Slew Rate	f_T
318	70V / μ sec	15MHz
741	0.5V / μ sec	1.2MHz

2.) Use the slew rate to calculate the rise and fall time of an output pulse whose amplitude is 10V. Draw a sketch of v_o for a 10kHz input square wave. Include these calculations in your laboratory report.

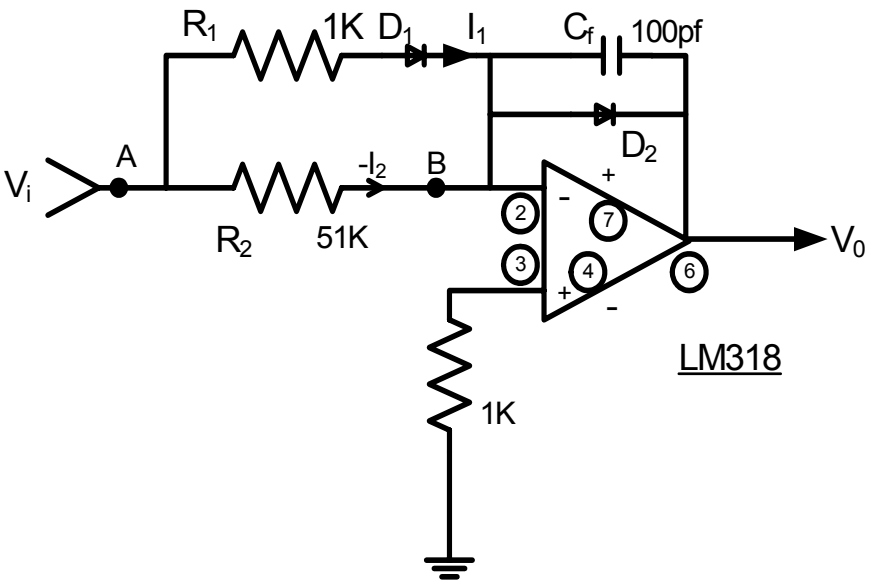
Do the following checks to ensure that the circuit is working before you begin the measurements in steps 3 and 4. When there is no input signal, V_o should be less than ± 0.1V. Measure the gain using a 1kHz sine wave.

3.) Use a 741 op-amp. It is good practice to observe the input and output signals simultaneously (GIL 4.3). Measure f_{bc} (GIL 5.6A). Be sure that the signal amplitude does not exceed the slew-limit in the frequency range you are using. After you measure f_{bc}, increase the size of the signal and observe the amplitude at which slew-rate distortion becomes evident. Next, use a 10k Hz square wave and adjust the signal amplitude so that $V_o(p-p)$ is approximately 10V. Measure the positive and negative slew rate from the scope face. You do no need to sketch v_o for the sine or square wave.

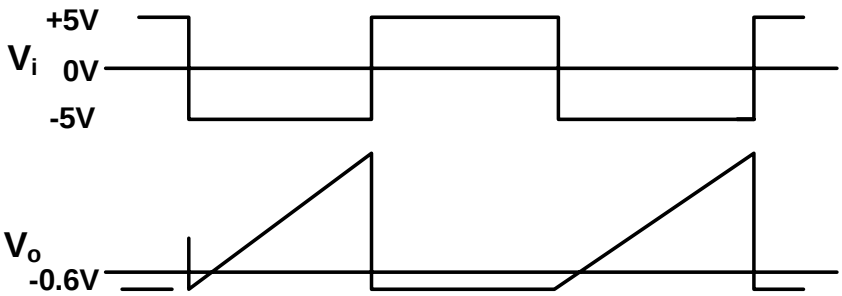
4.) Repeat step 3 for the 318. You should observe a large increase in the gain at the closed-loop break-frequency f_{bc}, which indicates that the phase shift of the 318 exceeds 90 degrees in this frequency range. You also see that the 318 has better high frequency gain than the 741. The slew rate of the 318 is so large that you probably cannot observe slew-rate distortion in this circuit. The output rise and fall for a square wave are much faster for the 318 than for the 741. Observe this fact, but it is not necessary to measure the slew rate or sketch v_o. You should also notice a damped overshoot on the output pulse, which is caused by the excess phase shift.

B. A Simple Ramp Voltage Generator

Op-amp rule II is applied in the following circuit. The input signal is a square wave applied at point A. Point B is a virtual ground (GR-II). $\pm$ 15V power supplies are used for all circuits.



When v_i is negative, the electrons that flow through R_2 are pulled into the feedback capacitor C_f by the op-amp. Diode-1 prevents current from flowing through R_1 during this part of the cycle. v_o rises at a constant rate as C_f is charged.



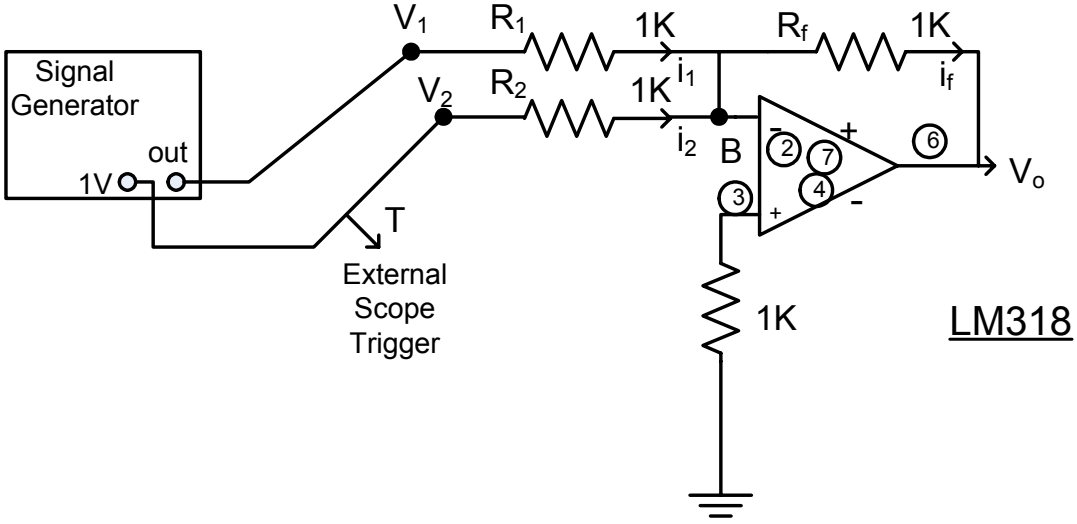
When v_i goes positive, a larger current flows through R_1 to discharge C_f rapidly. When v_o reaches-0.6V, diode-2 is forward biased, which causes I_1 to flow through D_2 rather than into C_f. Since no current is flowing into the capacitor at this time, v_o stays at –0.6V until v_i goes negative again. Then the cycle is repeated.

5.) Given that the input signal v_i is a 50kHz, 10V square wave (i.e. v_i switches between –5V and +5V). Calculate the slope and size of the ramp.

6.) Observe and sketch the waveforms described in step-5. Change the slope of the ramp by adjusting the amplitude of v_i. Change the length of the ramp by adjusting the period of v_i. Notice that if you make the v_o too large, the op-amp saturates, i.e. v_o is constant. Observe that v_o does not go below –0.6V.

C. Summing Circuit

Since point B in the following circuit is a virtual ground (GR-II), i_1 and i_2 are proportional to the two input signals v_1 and v_2. GR-II requires that the total input current ($i_1 + i_2$) must be pulled through R_f.



The signal generator is connected to the op-amp as shown in the sketch above. v_1 is a square wave and v_2 is the "1-volt" since wave from the generator. The peak value of V_2 is 0.7V because 1-volt is the RMS value and the output resistance is 1K, which causes a 50% attenuation. The 1-volt signal goes to the external trigger input of the scope through a T-connector before it goes to the circuit. Use the external scope trigger.

7.) Set the signal generator for 10kHz. Do not connect v_1 initially. Observe v_2 and v_o with a scope probe (or a cable with a clip lead). You should see that the circuit has a gain of –1. Move the scope probe from v_2 to v_1. Start small and increase v_1 until its amplitude is similar to v_2, while continuing to observe v_o. The output should be the sum of the two input waves. Vary the amplitude of v_1 as needed to understand the waveform at the output.

D. Reactance in the Feedback Loop. (You make skip section D if it will cause the lab to exceed 3 hours.)
A capacitor is included in the feedback loop of the following inverting amplifier. The parallel 100K resistor is needed to set the quiescent conditions. It does not affect the signal when $X_c << R$.

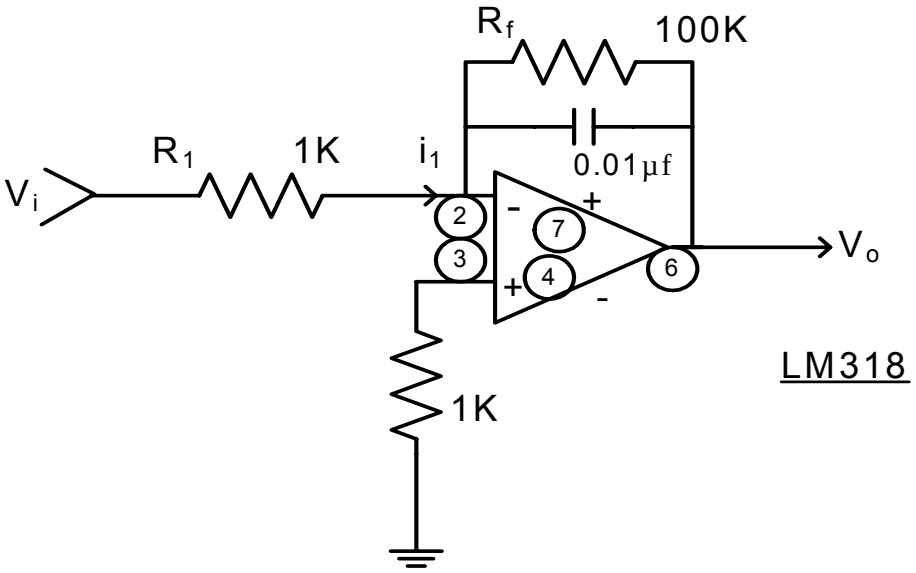


Figure 2

The usual gain equation applies except that the feedback path has reactance rather than a resistor.

$$\frac{v_o}{v_i} = -\frac{x_c}{R_1} = -\frac{-jX_c}{R_1} = -\frac{X_c}{R_1} \angle\text{-}90 \qquad (12.5)$$

8.) Calculate v_o / v_i for 1.6kHz and 16kHz sine waves. What is the phase shift between v_o and v_i?

9.) Return to internal triggering. Measure the gain of the amplifier for the two frequencies in step 8. Measure the phase shift at 1.6kHz (GIL-5.11). Since the amplifier inverts, compare the negative peak of v_o to the preceding positive peak of v_i.

A square wave input produces a triangle wave at the output. When v_i is positive, v_o is a negative ramp whose slope is determined by I_1 and the capacitor. Since v_i is symmetric around 0V, the positive and negative slopes are the same, producing a triangle wave.

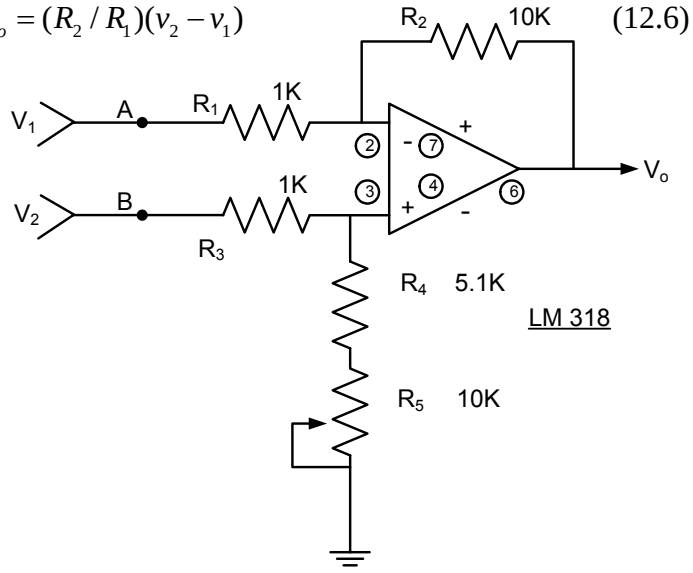
10.) Given that v_i is a 10V(p-p), 20kHz square wave, calculate the rate at which v_o changes. Draw a sketch of v_i and v_o including time and voltage scales.

11.) Observe the waveforms described in step 10. You can vary the period of the square wave and its amplitude to see the effect on the output. The triangle wave may not be symmetric around zero volts. That is, the whole wave may be on the positive (or negative) side of zero volts. In that case, the peaks of the wave can be flattened by saturation limits of the op-amp (approximately 13V).

E. Feedback Difference Amplifier

R_5 must be adjusted to make $R_3/(R_4+R_5)$ exactly equal to R_1/R_2. In that case, v_o will be zero when v_1 and v_2 are equal because v_- is equal to v_+. On the other hand when v_2 is zero, the circuit is simply an inverting amplifier with a gain of (R_2/R_1). Therefore the gain of this difference amplifier is:

$$v_o = (R_2/R_1)(v_2 - v_1) \qquad (12.6)$$



12.) Connect points A and B together and apply a 10V(p-p), 1kHz sine wave to them. Adjust R_5 until v_o is as small as possible (typically 10mV). In this differential mode there is minimal response at the output, although a large signal is applied to both inputs.

13) Connect point B to ground and apply a 1V signal to point A. You should see that the output signal is amplified by a factor of 10. Since the differential gain is 10, and the common-mode gain is 0.001, the common mode ratio is 10^4, or 80db.

F. Feedback Controlled Constant Current Source.

The output of the op-amp adjusts the gate voltage to keep the source of the FET at 0V, because the source is connected to the inverting input. The electrons flowing through R_1 must flow through the FET. The op-amp will adjust the gate voltage to let I_1 go through the FET even if there is a change in the drain voltage, hence this is an excellent constant source.

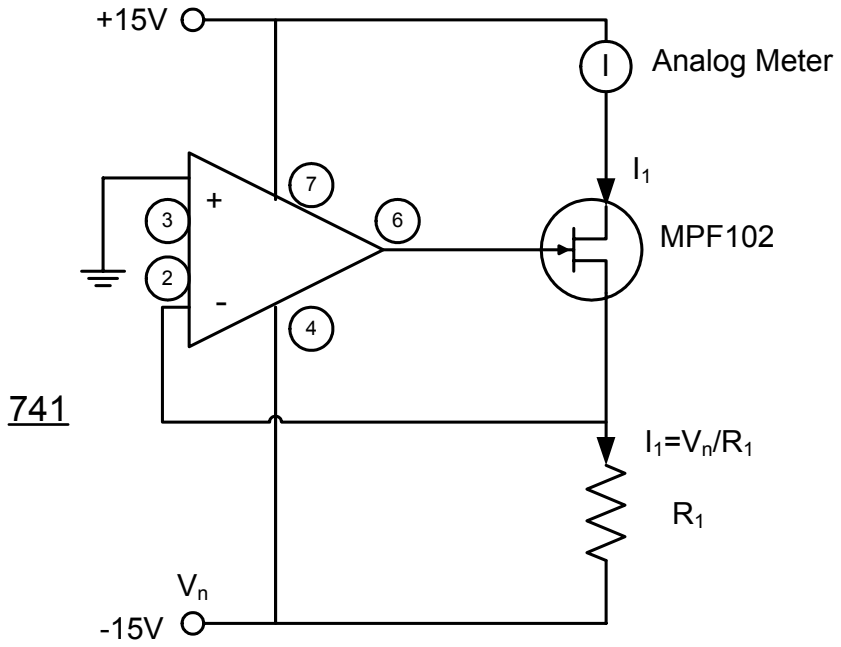


Figure 3

14.) Calculate the value of the drain current for R_1 equal to 150K and 15K. Assume that V_T is 2V and I_{dss} is 5mA. Calculate the gate voltage for the two resistor values.

15.) The analog meter is inserted in the drain lead to observe the FET current. Use the digital meter to measure the gate voltage relative to common. Measure I_d, V_g and V_s for the two resistors. Notice that the gate voltage is changed by the op-amp to let the current through, while keeping the source at 0V. When the 15K resistor is in the circuit, vary the positive supply voltage from +15 to +10V to see that the op-amp changes the gate voltage to let the same current flow through FET at the lower drain voltage. Notice that the source voltage stays at 0V, hence the current flowing through R_1 and the FET is constant.

COMPONENTS

Op-amp: 741
Capacitors: 2-0.1 μ f
Resistors: 4-1K, 1.1K, 10K

Please get the following components later if someone is waiting.

Devices: 318 op-amp, 2-1N914 diodes, MPF-102 FET
Capacitors: 100pf, 0.01 μ f
Resistors: 2K pot, 9.1K, 15K, 51K, 150K