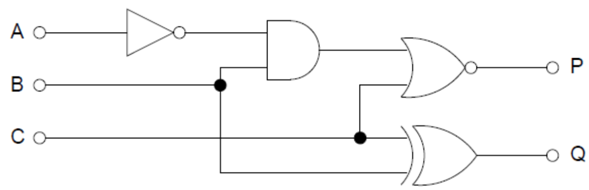
Physics 53600 Final Exam – May 7th 2020

Answer all six questions in a suitably formatted document that is to be sent by e-mail to jones105@purdue.edu no later than 8:00 am EDT on Friday, May 8th.

1. Consider the following digital logic circuit, which has three inputs and two outputs:

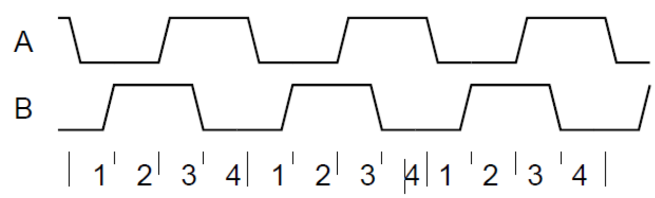


   (a) Write down the truth table for this logic circuit, showing the outputs P and Q for all possible values of the inputs, A, B, and C.
   (b) Find Boolean algebraic expressions for the outputs, P and Q, in terms of the inputs.
   (c) Draw an equivalent circuit that uses only 2-input AND gates and 2-input OR gates, with bubbles at the inputs of the AND gates to indicate where signals are inverted.

2. Describe the methods used to synchronize the sampling of data signals in the following communication methods:
   (a) A parallel printer port, consisting of data signals $D_{0..7}$ and a $\overline{STROBE}$ signal
   (b) A Serial Peripheral Interface (SPI), consisting of data lines $DIN/DOUT$ and a clock signal, $SCLK$.
   (c) An Inter-IC (IIC, or I2C) interface, consisting of a data signal, SDA, and a clock signal, $SCLK$.
   (d) A serial RS-232 data link
   (e) A high speed serial data link that uses data encoding and a clock-recovery circuit.

   What I'm asking is for you to describe how the signals can be used to determine the appropriate time to sample the data, such that it is guaranteed not to be in a state of transition.

3. Quadrature encoding is a technique used to determine the direction of rotary motion in the following way. Signals A and B are derived from an optical or magnetic sensor such that they are always 90° out of phase as shown:



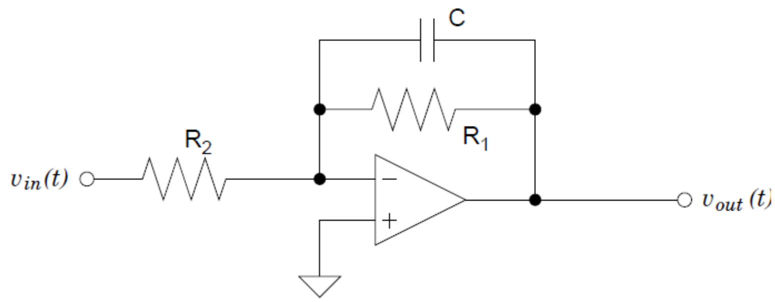
When rotation is clockwise, A and B have values corresponding to the phases 1,2,3,4, 1,2,3,4, … and when rotation is counter-clockwise, A and B have the values corresponding to phases 4,3,2,1, 4,3,2,1, …

(a) Write a table showing the values of A and B over at least 5 phases when rotation is clockwise. Write a second table for the case where rotation is counter-clockwise.

(b) Show how an edge-triggered D-type flip-flop can use signals A and B to provide a Boolean logic level that indicates whether rotation is clockwise or counter-clockwise, provided the angle of rotation exceeds 360°.

(c) Using A and B to represent the values in the previous phase, and A' and B' to represent the values in the current phase, write Boolean algebraic expressions for signals CW and CCW that are true when the rotation is clockwise or counter-clockwise, respectively.

4. Consider the following circuit:

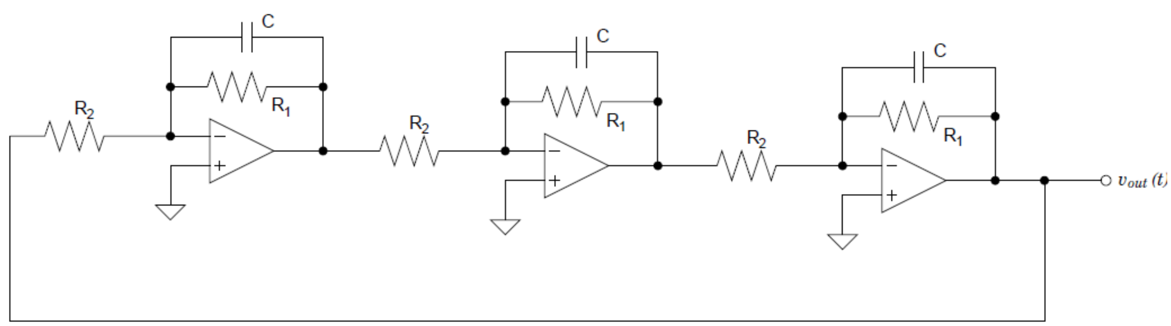


(a) If $v_{in}(t) = V_{in}e^{i\omega t}$, calculate the magnitude and relative phase of $v_{out} = V_{out}e^{i\omega t}$ as a function of frequency, ω. If V_{in} is a real number, indicate which quadrant of the complex plane V_{out} lies in.

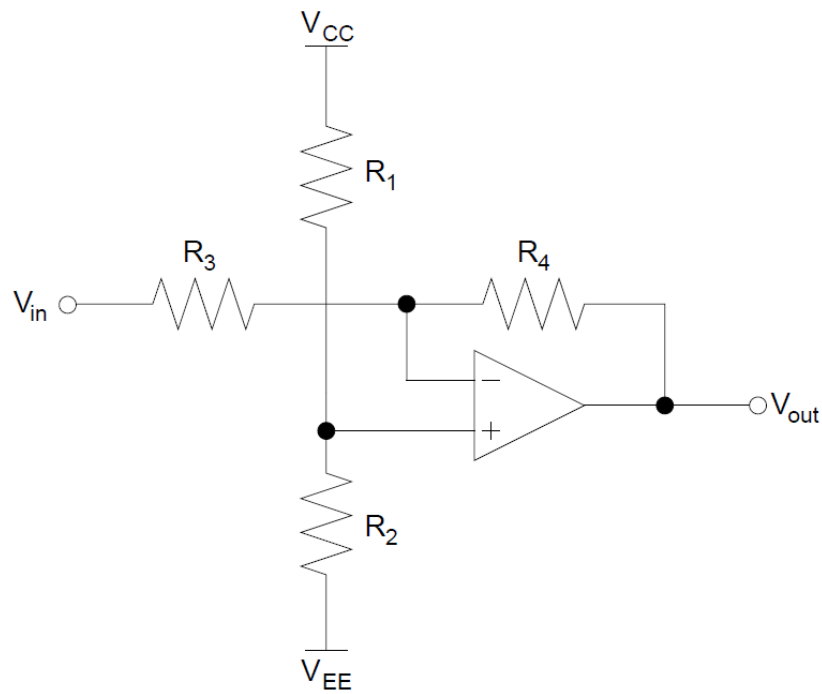
(b) If $C = 27.5\ nF$ and $R_1 = 1\ k\Omega$, at what frequency will the phase shift reach 120°? Hint: $\tan 120° = \sqrt{3}$ and $\sqrt{3}/2\pi$=0.275.

(c) What value of R_2 will yield a voltage gain with a magnitude of one at this frequency?

(d) Describe the waveform, v_{out}, in the following circuit, where the component values re those determined above:



5. Consider the following operational amplifier circuit:



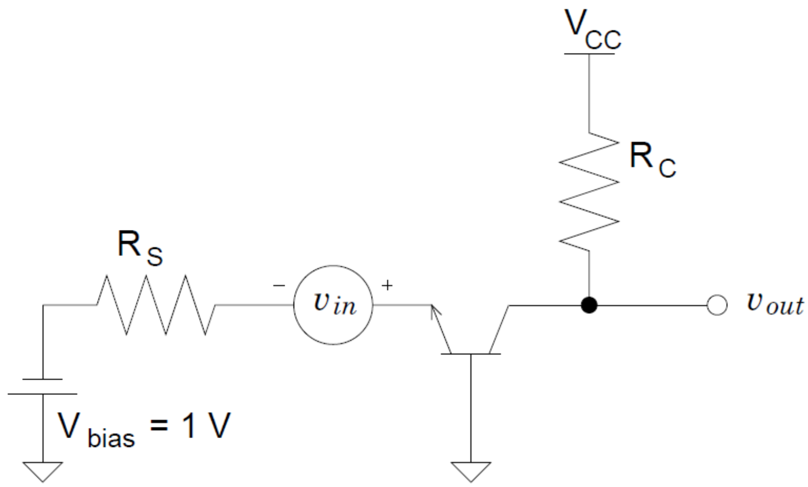
(a) Derive constraints that R_1, R_2 and R_3, R_4 must satisfy in order to implement the following linear transformation of the input voltage:

$$v_{out} = (-1.0\ V) - \frac{v_{in}}{5}$$

(b) Calculate component values that will work, given the following additional assumptions:

- $V_{CC} = +5\ V$
- $V_{EE} = -5\ V$
- The current through R_1, R_2 should be about 1 mA
- The current through R_4 should not be more than about 1 mA for $V_{CC} > v_{in} > V_{EE}$

6. The following circuit has a transistor connected in the "common base" configuration:



(a) What is the voltage at the emitter and what current flows out of the emitter expressed in terms of V_{bias}, R_S, v_{in}, and V_{be}?
(b) Express the small signal voltage gain in terms of the resistances, R_S and R_C.
(c) Why would you expect this circuit to have better high frequency response than a common-emitter amplifier?