Physics 53600 – Assignment #4 Solutions

1. The 2N3819 JFET has a pinch-off voltage of $V_P = -3\ \mathrm{V}$ and a drain-source saturation current of $I_{DSS} = 11.7\mathrm{mA}$. When biased in the active region, the drain current is then given by

$$I_D = I_{DSS}\left(1 + \frac{V_G}{|V_P|}\right)^2$$

   (a) What value of V_G will produce a constant drain current of 5 mA?

This is just straight-forward algebra where we solve for V_G:

$$V_G = |V_P|\left(\sqrt{\frac{I_D}{I_{DSS}}} - 1\right) = -1.039\ V$$

   (b) Determine the values of R_1 and R_2 that will result in a voltage divider between $V_{DD} = +5\ V$ and $V_{SS} = -5\ V$ that produces the gate voltage determined in part (a) and has an impedance of $100\ k\Omega$. Consult the solutions to the midterm exam for an example.

From the solutions given to the midterm, we can use the formulas:

$$V_{out} = \frac{V_{CC}R_2 + V_{EE}R_1}{R_1 + R_2}$$

$$Z = \frac{R_1 R_2}{R_1 + R_2}$$

from which we can get

$$R_1 = Z\left(\frac{V_{CC} - V_{EE}}{V_{out} - V_{EE}}\right)$$

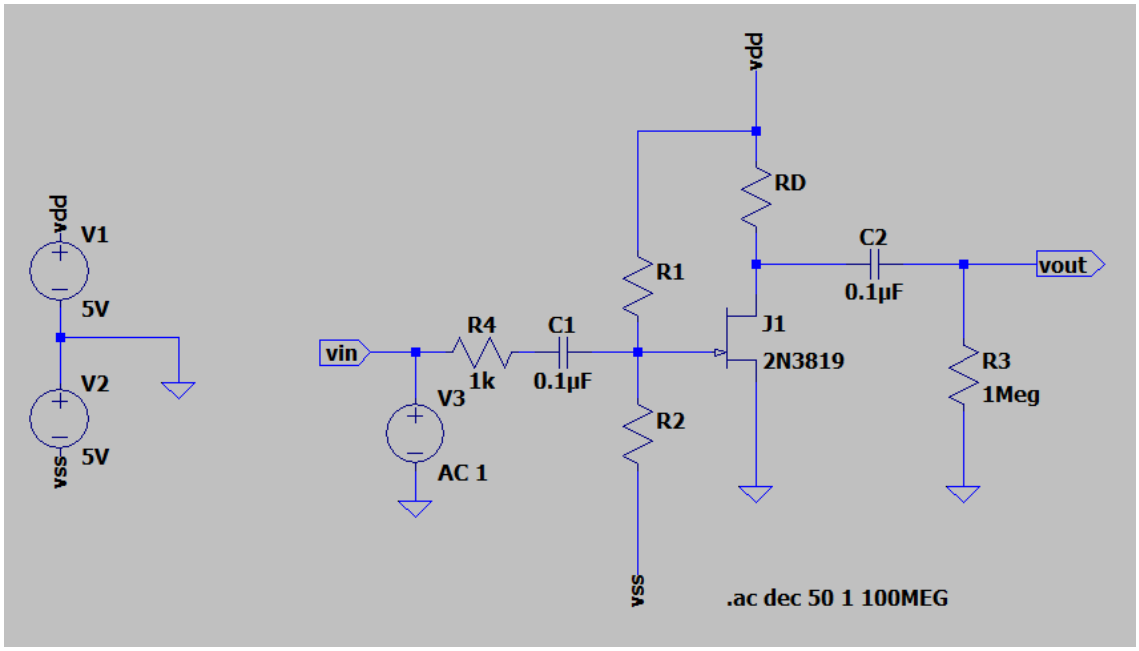
$$R_2 = Z\left(\frac{V_{CC} - V_{EE}}{V_{CC} - V_{out}}\right)$$

Here, it is assumed that R_1 is connected to V_{CC} and R_2 is connected to V_{EE}. Using these equations, you can calculate:

$$R_1 = 252\ k\Omega$$

$$R_2 = 166\ k\Omega$$

(c) Consider the following circuit, in which R_4 represents the finite output impedance of a signal to be amplified.



what value of R_D will produce a small-signal voltage gain of $A = 3$?

Well technically the question should have been asking for a gain of $A = -3$ because this is an inverting amplifier configuration. Since the current into the drain is

$$I_D = I_{DSS}\left(1 + \frac{V_G}{|V_P|}\right)^2$$

a small change in V_G results in a corresponding small change in I_D which is given by

$$\delta I_D = 2\frac{I_{DSS}}{|V_P|}\left(1 + \frac{V_G}{|V_P|}\right)\delta V_G$$

and the small variation in the output voltage will be

$$\delta V_{out} = -R_D \delta I_D.$$

Thus,

$$R_D = -\frac{\delta V_{out}}{\delta I_D} = -\frac{\delta V_{out}}{\delta V_G}\left(2\frac{I_{DSS}}{|V_P|}\left(1 + \frac{V_G}{|V_P|}\right)\right)^{-1}$$
$$= -A\left(2\frac{I_{DSS}}{|V_P|}\left(1 + \frac{V_G}{|V_P|}\right)\right)^{-1}$$
$$= 588\ \Omega$$

(d) Simulate the circuit using both a DC operating point and an AC frequency sweep analysis. Identify in the simulation output the quiescent drain current, the gate voltage, and the voltage gain at moderate frequencies of ~10 kHz.

Here are the results of the DC operating point analysis:

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--- Operating Point ---

V(n001):        2.01724         voltage
V(n003):        -1.02871        voltage
V(vss):         -5              voltage
V(vdd):         5               voltage
V(n002):        -1.02871e-015   voltage
V(vin):         0               voltage
V(vout):        2.01724e-012    voltage
I(C2):          -2.01724e-018   device_current
I(C1):          -1.02871e-018   device_current
Id(J1):         0.0050641       device_current
Ig(J1):         -5.09349e-012   device_current
Is(J1):         -0.0050641      device_current
I(R4):          -1.02871e-018   device_current
I(R3):          2.01724e-018    device_current
I(R2):          2.39234e-005    device_current
I(R1):          2.39234e-005    device_current
I(Rd):          0.0050641       device_current
I(V3):          -1.02871e-018   device_current
I(V1):          -0.00508802     device_current
I(V2):          -2.39234e-005   device_current
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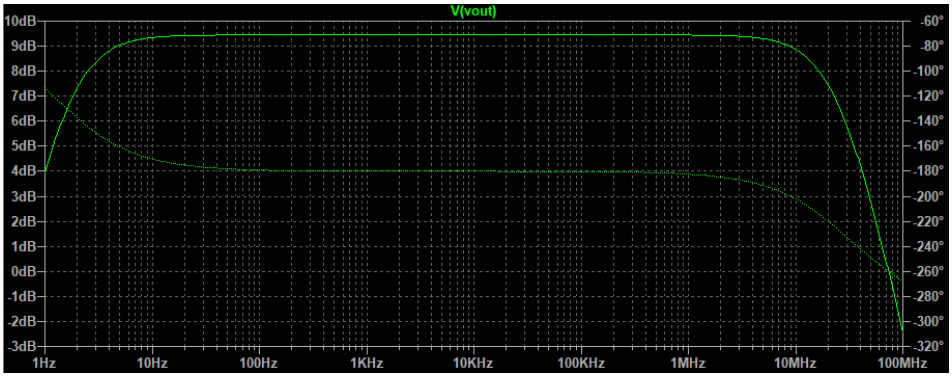
Gate voltage

Drain current



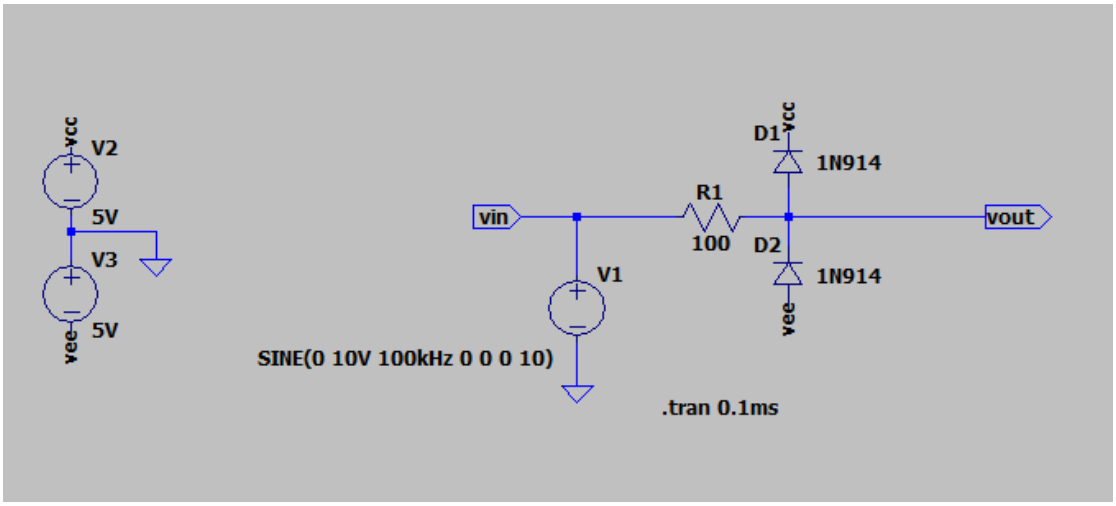
This shows that at moderate frequencies (eg. 10 kHz) the voltage gain is 9.45 dB. Using the definition. Using the definition

$$G = 20 \log_{10} A$$

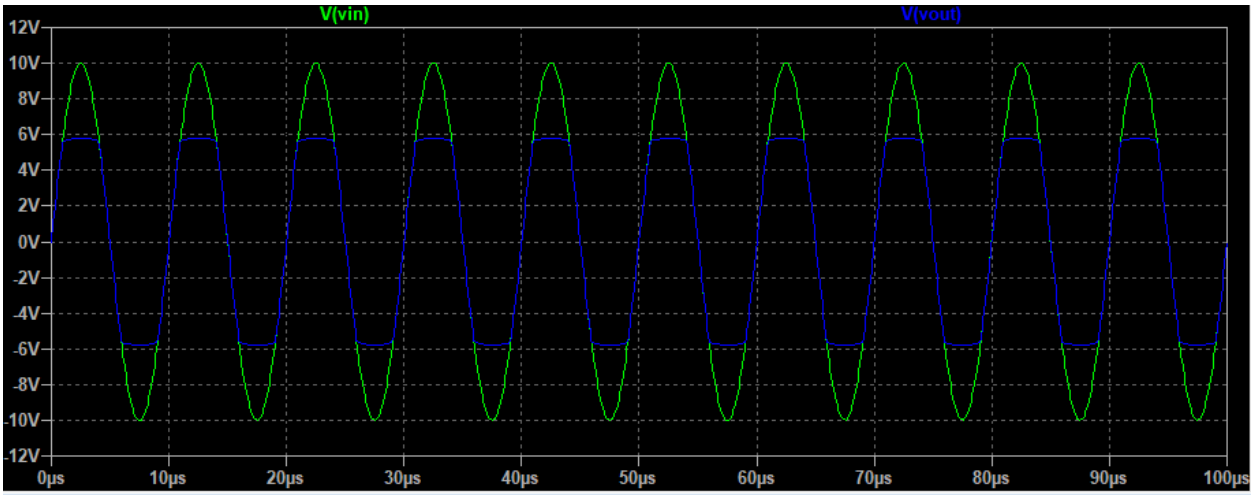
this confirms that

$$A = 10^{G/20} = 2.97 \approx 3$$

2. A diode clamp circuit can be used to limit the range of input voltages to a sensitive circuit. Using 1N914 silicon diodes, simulate the following circuit and demonstrate that the voltage at the node V_{out} has been limited and identify what the limiting voltage range is.

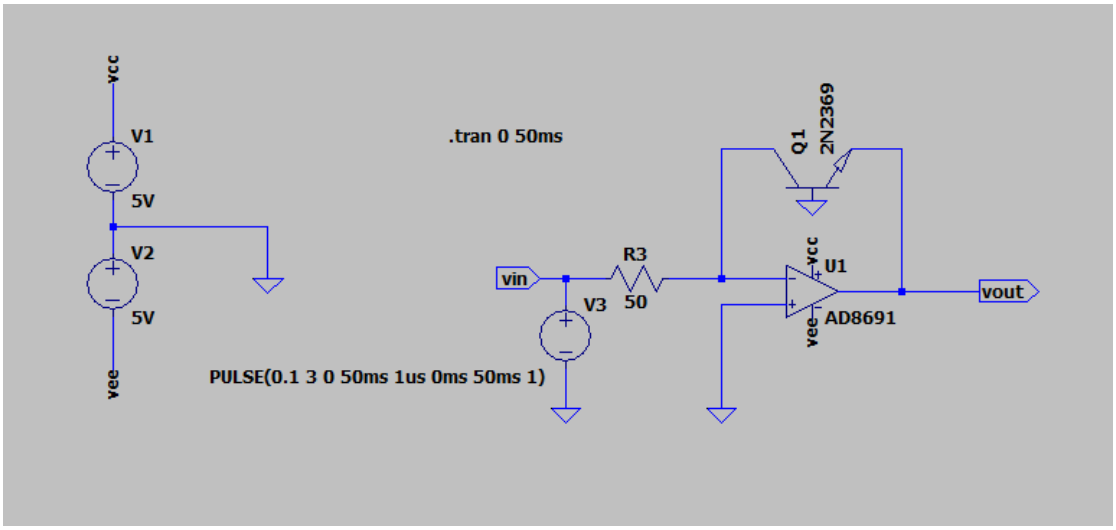


Here is the output of the simulation:



which shows that the voltage has been limited to about $\pm 5.7\ V$.

3. The following circuit is a logarithmic amplifier:



(a) What is the output voltage when the input voltage is 0.1 V?

From the DC operating point simulation of this circuit, it can be determined that the output voltage is $v_{out} = -0.635\ V$ when the input voltage is $v_{in} = 0.1\ V$.

(b) What is the output voltage when the input voltage is 3 V?

Again, the DC operating point simulation determines that $v_{out} = -0.736\ V$ when $v_{in} = 3\ V$.

(c) Design a second state operational amplifier circuit, configured as an inverting summing amplifier that produces an output of 0V when the input voltage is 0.1 V and an output voltage of 1 V when the input voltage is 3 V.

An inverting, summing amplifier, like the one shown on page 6 of Lecture 14, provides an output voltage that is related to the input voltages as follows:

$$v_{out} = -R_F\left(\frac{v_1}{R_1} + \frac{v_2}{R_2}\right)$$

In this case, we can select $R_1 = R_2$ to obtain

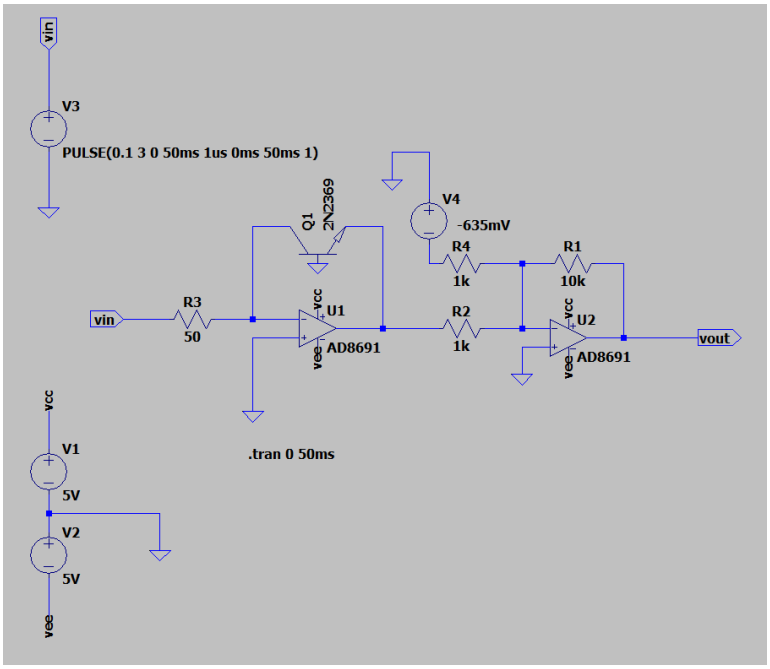
$$v_{out} = -\frac{R_F}{R_1}(v_1 + v_2)$$

where v_1 is the output of the logarithmic amplifier and v_2 is a constant voltage source that will satisfy the specified requirements. In this case, $v_2 = +0.635\ V$ so that $v_{out} = 0\ V$ when $v_{in} = 0.1\ V$. Next, when $v_{in} = 3\ V$, the output of the logarithmic amplifier would be $v_1 = -0.736\ V$ and

$$v_{out} = -\frac{R_F}{R_1}\big((-0.736\ V) + (0.635\ V)\big) = -\frac{R_F}{R_1}(-0.101\ V) = 3\ V$$

Thus, the ratio of resistances must be 10. A reasonable choice would be to use $R_F = 10\ k\Omega$ and $R_1 = 1\ k\Omega$.

The required circuit is shown below, although some of the resistor labels are different from what has been described previously.



with the following simulation output: