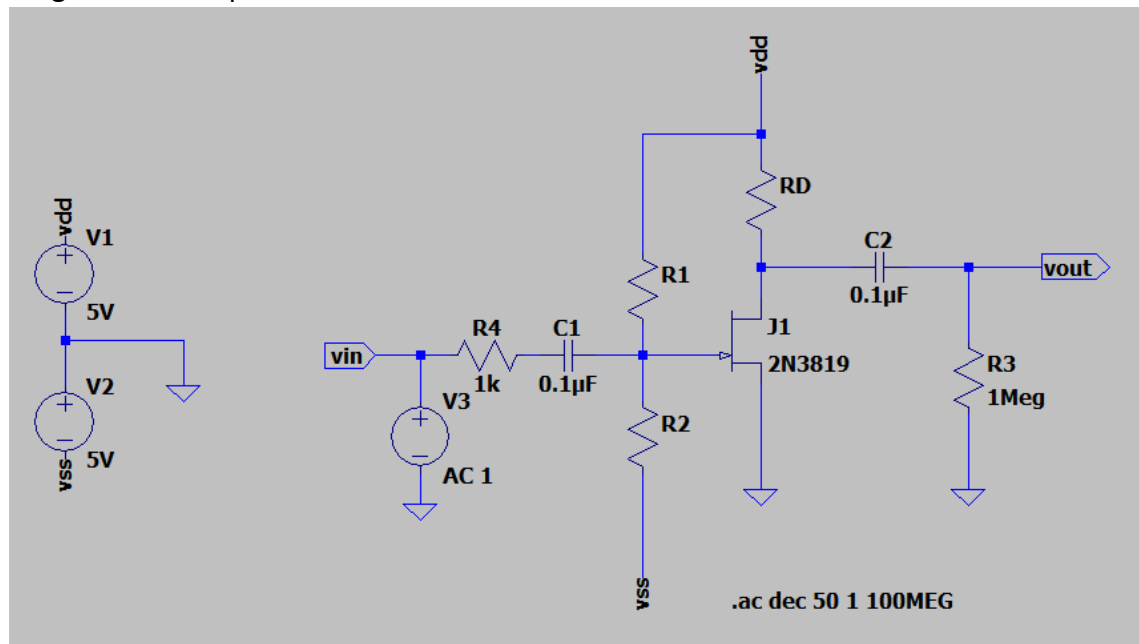


## Physics 53600 – Assignment #4 – Due March 26, 2020

1. The 2N3819 JFET has a pinch-off voltage of  $V_P = -3\text{ V}$  and a drain-source saturation current of  $I_{DSS} = 11.7\text{ mA}$ . When biased in the active region, the drain current is then given by

$$I_D = I_{DSS} \left( 1 + \frac{V_G}{|V_P|} \right)^2$$

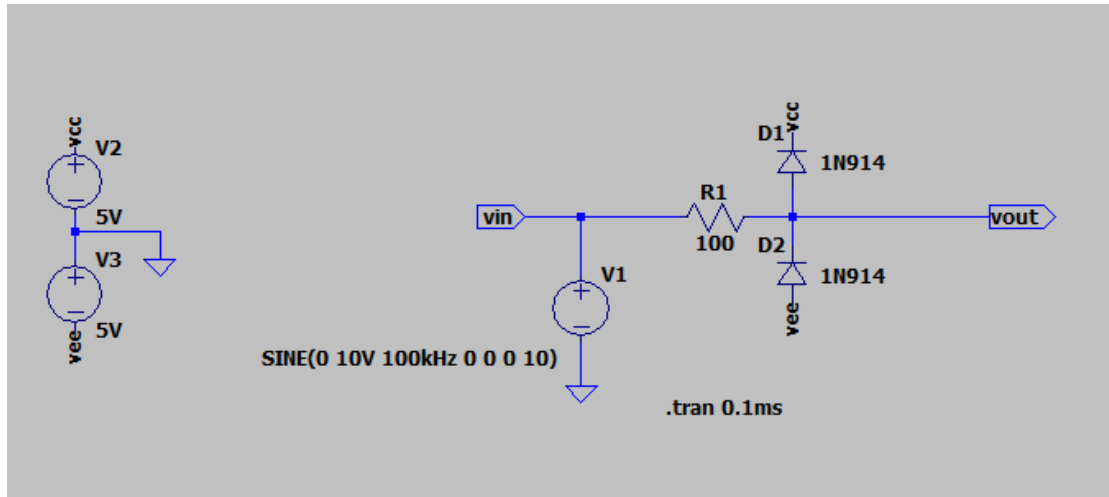
- (a) What value of  $V_G$  will produce a constant drain current of 5 mA?
- (b) Determine the values of  $R_1$  and  $R_2$  that will result in a voltage divider between  $V_{DD} = +5\text{ V}$  and  $V_{SS} = -5\text{ V}$  that produces the gate voltage determined in part (a) and has an impedance of  $100\text{ k}\Omega$ . Consult the solutions to the midterm exam for an example.
- (c) Consider the following circuit, in which  $R_4$  represents the finite output impedance of a signal to be amplified.



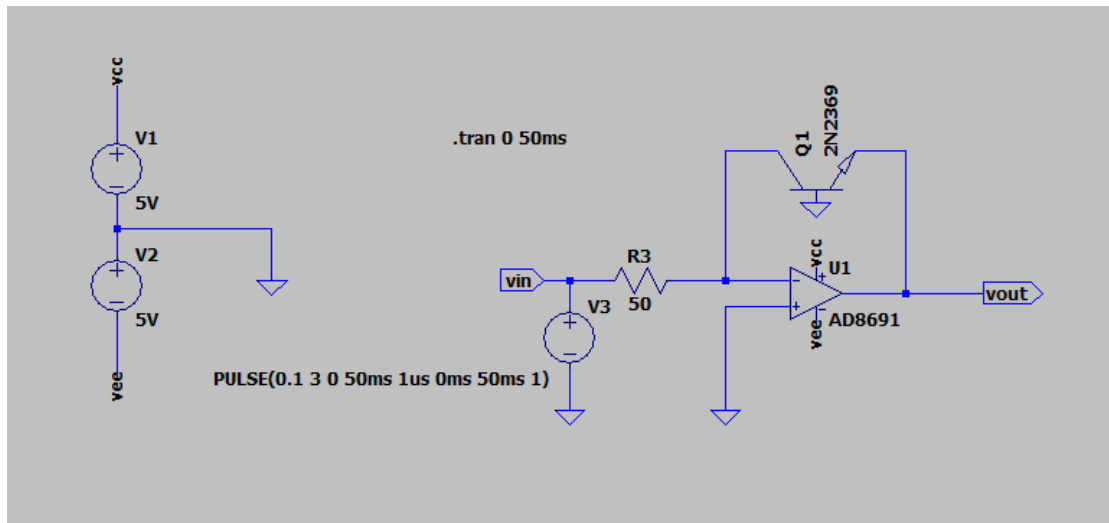
what value of  $R_D$  will produce a small-signal voltage gain of  $A = 3$ ?

- (d) Simulate the circuit using both a DC operating point and an AC frequency sweep analysis. Identify in the simulation output the quiescent drain current, the gate voltage, and the voltage gain at moderate frequencies of  $\sim 10\text{ kHz}$ .

2. A diode clamp circuit can be used to limit the range of input voltages to a sensitive circuit. Using 1N914 silicon diodes, simulate the following circuit and demonstrate that the voltage at the node  $V_{out}$  has been limited and identify what the limiting voltage range is.



3. The following circuit is a logarithmic amplifier:



- What is the output voltage when the input voltage is 0.1 V?
- What is the output voltage when the input voltage is 3 V?
- Design a second state operational amplifier circuit, configured as an inverting summing amplifier that produces an output of 0V when the input voltage is 0.1 V and an output voltage of 1 V when the input voltage is 3 V.