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Surface Gate-Defined Quantum Dots in MoS_2 with Bi Contacts

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Transition-metal dichalcogenides (TMDCs) are promising materials for nano and quantum devices, with performance dependent on electrical contacts and gate electrodes at cryogenic temperatures. In this study, we utilized semimetal bismuth as the contact metal to fabricate two types of devices based on MoS_2-Bi: field-effect transistors (FETs) and quantum dot devices. We observed linear current–voltage characteristics in the FET devices at temperatures of 4.2 and 0.4 K, within the range of −0.03 to 0.03 V, essential for quantum devices. For the MoS_2 quantum dot device, we utilized intrinsic Schottky barriers between MoS_2 and gold as gate electrodes to form and control the quantum dots. Coulomb diamonds were observed in the MoS_2 devices at temperature of 0.4 K, with extracted parameters matching our device design. Our simplified fabrication process eliminates the need for additional fabricate gate insulators steps, enhancing design flexibility and fabrication possibilities for advanced quantum devices, including vertically integrated systems.

1. Introduction

The increasing demand for faster and more powerful computational techniques has driven researchers to explore the atomic level and use quantum mechanical systems for information processing. Following the development of quantum dot devices in graphene[1–3] and bilayer graphene,[4–9] the search for similar realizations in other two-dimensional (2D) materials has led to the discovery of transition metal dichalcogenides (TMDCs) as promising candidates for quantum devices, particularly molybdenum sulfide MoS_2.[10–13] These TMDC materials are bonded by van der Waals (vdW) forces between individual layers.[10,14–16] In terms of electronics, carriers in TMDCs can be controlled by electric potentials, making them suitable for device applications such as field-effect transistors (FETs).[17–20] The distinct properties of 2D TMDCs, including high mobility,[21] spin and valley physics,[22–26] long spin coherence time[27] and large spin–orbit coupling,[28] make them potential candidates for quantum information and computation.[29,30]

However, the Schottky barriers between the contact metals and TMDCs induce a high contact resistance at cryogenic temperatures,[31] which hinders many applications, including quantum devices. These contacts in TMDCs are influenced by the band structures of the semiconductor and metal owing to metal- and disorder-induced gap states.[32] These problems are commonly referred to as Fermi-level pinning. To date, many efforts have been made to solve this issue by exploring new materials[33–37] and inserting an ultrathin interlayer.[38–40] Here, a semimetal is expected to be a good candidate material because of its low density of states, reaching nearly zero around the Fermi level. Consequently, it suppresses the metal-induced gap states and contributes to gap state saturation. Recently, no barrier formation and low contact resistance have been reported in TMDCs monolayers with semimetal contacts.[41,42] In particular, bismuth contacts exhibit these characteristics at temperatures as low as 77 K.[41] This suggests the usefulness of Bi contacts not only in electronics but also in potential quantum device applications. However, studies on quantum devices remain limited.[43]

Electrical contacts operating under cryogenic and low-bias conditions are essential for quantum devices. The typical bias voltage in quantum devices is within the range of a few millivolts,[2–13,15,43–47] many previous studies focused on current–voltage characteristics extending up to approximately 1 V,[19–21,31,33–37,39–42,48] resulting in a lack of detailed discussion of the low-bias region. Therefore, it is necessary to investigate the effects of contact metals on the transport properties of TMDCs under these conditions, particularly from the perspective of quantum device applications.

In this study, we fabricated two types of multilayer MoS_2 devices with Bi/Au contacts: FETs and quantum dot structures. We conducted two-probe measurements, demonstrating the linear current–voltage characteristics of the FET devices in the low-bias region and at cryogenic temperatures. Additionally, we fabricated gate electrodes utilizing the intrinsic Schottky barriers formed at the interface between the pre-patterned Ti/Au gate electrodes and the transferred MoS_2. Using these structures, we observed Coulomb diamonds, indicating the formation of quantum dots, at temperature of 0.4 K.

2. FET Structure

2.1 *Device fabrication*

Multilayer MoS_2 thin flakes used in this experiment were exfoliated from a bulk crystal onto PDMS and then transferred to Si/SiO_2 substrates. The thickness of SiO_2

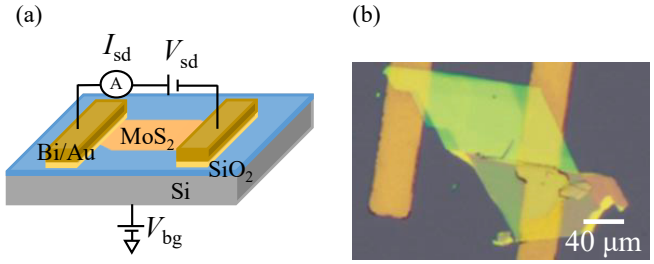

Fig. 1. (Color online) (a) Schematic of the MoS_2-Bi/Au based FET device structure. (b) Optical microscope image of the device.

was 285 nm. The thickness of the MoS_2 flakes was initially identified using an optical microscope based on color contrast and further confirmed to be approximately 5 nm using atomic force microscopy. The carriers induced by the back gate may be confined to a thickness smaller than that of the flake. The schematic of the MoS_2-based FET device geometry used for the two-probe measurements is shown in Fig. 1(a). We transferred MoS_2 flakes from PDMS to Si/SiO_2 and prepared contact electrodes using photolithography. We used semimetal bismuth to form the top source and drain contact electrodes. A thermal evaporator was utilized to deposit 40 nm of bismuth under high-vacuum conditions of 10^{-6} Torr to minimize interfacial contamination, followed by a 60 nm gold capping layer to prevent oxidation of bismuth. An optical microscopy image of the fabricated device is shown in Fig. 1(b).

2.2 *Current–voltage characteristics*

Two-probe measurements were conducted for electrical characterization of the fabricated MoS_2 devices at room temperature (RT). A typical drain current I_{sd} versus the source bias voltage V_{sd} characteristic for different global back-gate voltages V_{bg} (from −20 to 20 V) is shown in Fig. 2(a). With increasing V_{bg}, carriers (electrons) were induced, and an increase in conductance was observed. When the conduction channel was opened, a linear slope of I_{sd}–V_{sd} characteristics was observed, with V_{sd} ranging from −0.03 to 0.03 V, as shown in Fig. 2(b), which increases with V_{bg}.

Next, we measured the electron transport at low temperatures. 2D color maps of the measured I_{sd} as a function of V_{sd} and V_{bg} in the MoS_2 device at 4.2 K are shown in Fig. 2(c). We observed the opening of the conduction channel by applying a positive V_{bg}. Figure 2(d) shows the drain current I_{sd} versus source bias voltage V_{sd} characteristics for different back-gate voltages V_{bg} (from −20 to 20 V). We also observed linear I_{sd}–V_{sd} characteristics, with V_{sd} ranging from −0.03 to 0.03 V. A previous study,[43] which measured MoS_2 nanotubes and nanoribbons, made it challenging to discuss the effects of Bi contacts on linearity owing to the formation of built-in quantum dots at temperature of 20 mK. Hence, the observed linearity in our device is purely reflective of the effect of the bismuth contacts, which has not been previously reported at cryogenic temperatures. These results are promising for measuring quantum transport properties.

3. Quantum Dot Structure

3.1 *Device fabrication*

In this study, we developed gate electrodes to form

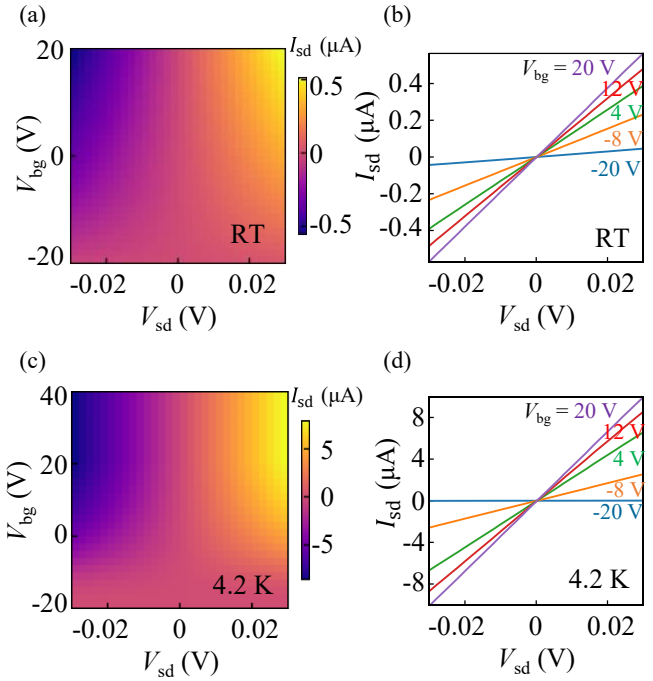

Fig. 2. (Color online) (a) Color map of the source–drain current in the device at RT. (b) The measured current as a function of source–drain bias and gate voltages in the MoS_2 device at RT. (c, d) Results conducted at 4.2 K.

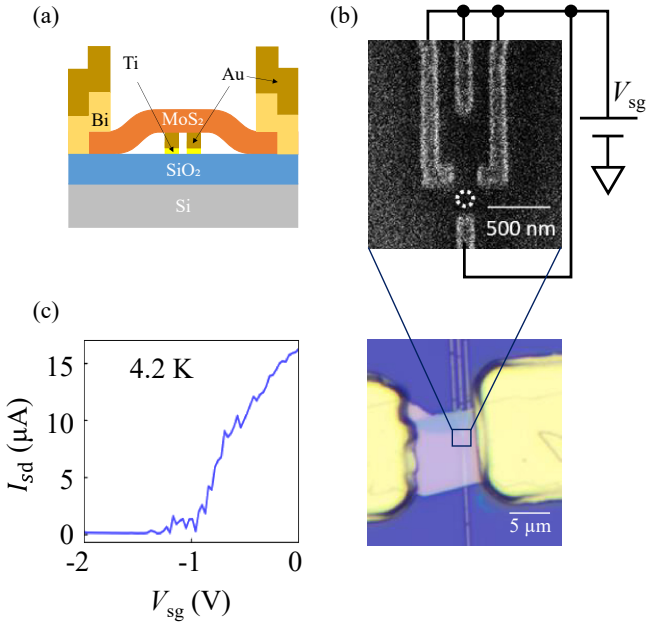

Fig. 3. (Color online) (a) Schematic layer structure of the MoS_2 quantum dot device utilizing intrinsic Schottky barriers between gold and MoS_2. (b) SEM image of pre-patterned Ti/Au fine gates to form a quantum dot. (c) The observed pinch-off property by the surface gates. V_{sg} is commonly applied to all of the surface gates.

confinement potentials for quantum dots. We utilized the intrinsic Schottky barriers formed at the interface between the gate electrode metal and MoS_2. Figure 3(a) illustrates the cross-sectional structure of the device. The gate electrodes were prepared using electron beam (EB) lithography on a Si/SiO_2 substrate. Titanium (10 nm) and gold (100 nm) were deposited by EB evaporation. Figure 3(b) shows a scanning electron micrograph of the fine gates and an optical

microscopy image of the device. Subsequently, a multilayer MoS_2 flake with a thickness of 50 nm, as evaluated by atomic force microscopy, was placed on top of the fine gates using the dry transfer technique[49] and treated with chloroform and hydrogen to further clean the elvacite residues. Such transfer interfaces are known to alleviate Fermi-level pinning compared to those created by evaporation, consequently leading to improved Schottky barrier characteristics, known as the S-value. Various metal/MoS_2 contacts with transfer interfaces were investigated in a previous study.[50] The I_{sd}–V_{sd} characteristics, which reflect the work function of each metal, are obtained. Specifically, the difference between the work function of gold and the electron affinity of MoS_2 is approximately 0.5 eV, and Schottky barriers close to this value have been demonstrated.[50] We utilized the fine gates as gate electrodes (referred to below as "surface gates", without any gate dielectric) to form the confinement potential of the quantum dot. After transferring MoS_2, top contacts (Bismuth: 40 nm and gold: 60 nm) were deposited using another round of photolithography followed by a thermal evaporation process.

Figure 3(c) shows the observed I_{sd} as a function of the surface gate voltage V_{sg} at 4.2 K. V_{sg} was applied to all surface gates. We set $V_{bg} = 80$ V to induce carriers in the MoS_2 device, and $V_{sd} = 10$ mV. The thickness of the conduction layer in MoS_2 induced by V_{bg} is approximately 10 nm from the substrate side.[51,52] This conduction layer can be controlled and depleted using a Schottky barrier. We observed the pinch-off property of the conduction channel at approximately −1.2 V. Schottky gates operate, depleting the conduction channel in MoS_2 around this surface-gate voltage range. While conventional gates for quantum devices require an insulator, such as *h*-BN, between the channel (such as TMDCs) and the gates,[11] our devices do not require it because the depletion layer acts as an effective insulator. Steepening of the confinement potential may also be expected by removing the insulator layer, enabling us to define smaller quantum dots.

3.2 *Formation of quantum dots*

Finally, we formed a quantum dot using fine-surface gates. The 2D color map of the observed differential conductance $\frac{dI_{sd}}{dV_{sd}}$ as a function of V_{sd} and V_{sg} is shown in Fig. 4. The conductance is suppressed around zero source–drain bias, and the width of the blocked region is modulated by V_{sg}. This corresponds to Coulomb diamonds, and their sizes are not uniform, indicating the formation of a quantum dot. The diamonds are closed at zero bias under resonant tunneling conditions, and the size of the diamond changes, reflecting the effect of the orbital levels formed in the dot. Note that we also observed other Coulomb diamonds under different gate bias conditions. We did not observe clear excitation lines from the orbital levels in our measurements, probably because of the relatively strong coupling between the dots and leads. From the smallest diamond, we extracted the charging energy $E_c = 0.9$ meV. This charging energy corresponds to a total capacitance of the quantum, $C = 180$ aF. We determined the capacitance between the surface gates and the quantum dot to be 30 aF.[44] These values are consistent with the device geometry, assuming a dot size ≈ 30 nm and a depletion layer thickness ≈ 1 nm, indicating

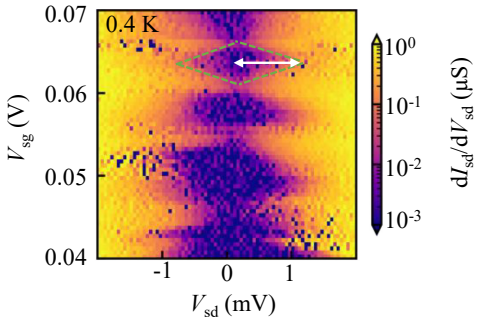

Fig. 4. (Color online) Observed differential conductance as a function of the source–drain bias and the surface gate voltages. Coulomb diamonds are observed. We use the smallest one indicated by a green dashed line for the analysis.

that a quantum dot is formed in the gap between the surface gates [indicated by a circle in Fig. 3(b)]. Surface charge impurities and the bending of the MoS_2 band may also contribute to the confinement potential of the quantum dot. Additionally, we found the capacitances between the quantum dot and the source (drain) electrodes, C_s and C_d, to be 92 and 57 aF, respectively. The parameters characterizing the quantum dots in this study are consistent with the previous findings.[11,53]

This approach offers design flexibility, which is advantageous for forming multiple quantum dots in future highly integrated and complex devices. For instance, vertically integrated quantum dots are expected to enable the realization of high-sensitivity charge sensors, facilitating the detection of ultrafast quantum dynamic phenomena.[45–47]

4. Conclusion

In conclusion, we fabricated two types of multilayer MoS_2 devices with Bi/Au contacts: FETs and quantum dots structures. For the FET structure, linear current–voltage characteristics were observed at both room and cryogenic temperatures of 4.2 K. Surface gate electrodes, utilizing the intrinsic Schottky barrier between the metal and MoS_2, effectively form quantum dots, allowing the removal of an insulator from the devices. This technique is simpler than traditional methods that involve gate insulators and post-EB lithography after the transfer of MoS_2. This simplification is advantageous for fabricating complex quantum devices, such as vertically integrated systems. Our findings with layered MoS_2 pave the way for exploring novel quantum effects, including spin-valley coupling and the manipulation of qubit systems.

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Appendix A: Results at 0.4 K

We also present the results from another device measured at 0.4 K [Figs. A·1(a) and A·1(b)]. Even if the temperature is lowered to 0.4 K, the device continues to exhibit near-linear

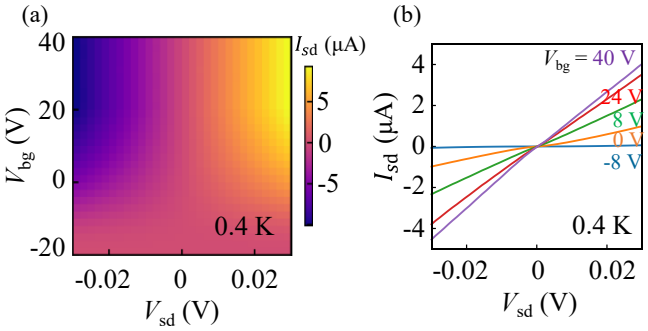

Fig. A·1. (Color online) (a) Color map of the source–drain current in the device at 0.4 K. (b) Current–voltage relation at different V_{bg}.

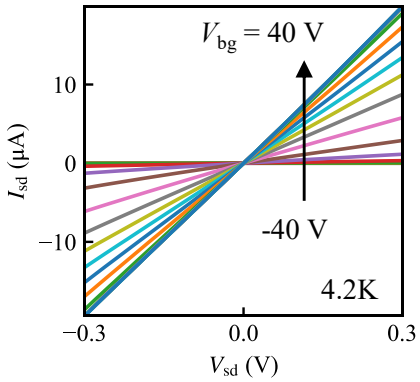

Fig. B·1. (Color online) Measured current as a function of higher source–drain bias, from −0.3 to 0.3 V, and gate voltage in the MoS_2 device at 4.2 K.

behavior. Please note that a different sample was used here compared to the one discussed in the main text.

Appendix B: Higher Bias Measurement

Figure B·1 shows the measured current over a higher V_{sd} range from −0.3 to 0.3 V. Linearity is also observed in the V_{sd} range. Please note that we used a different sample instead of the ones used in Figs. 2 and A·1.

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