

# High Mobility Ambipolar Field Effect Transistors Made From Large-Scale CVD Graphitic Thin Films

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Ultrathin graphitic films containing only one or a few graphene layers<sup>1,2</sup> have received great attention as a promising channel material to make “carbon-based” transistors<sup>1-3</sup>, particularly for high speed and/or low power electronic devices<sup>3-5</sup>. Back-gated or front-gated graphene field effect transistors (GFET) made from exfoliated (from bulk graphite) or epitaxially-grown (by surface decomposition of SiC) graphene layers can show electron *and* hole mobilities approaching  $10^4$  cm<sup>2</sup>/Vs or higher. Recent works have also shown that *ambipolar* GFETs with even rather low on-off ratio and mobilities can already be very valuable for rf applications<sup>4,5</sup>.

High quality graphene layers grown by CVD or related surface segregation on metals have been known for decades<sup>6</sup>. Only recently have few-layer graphitic films grown by such methods been transferred to insulators<sup>7</sup>, enabling electronic applications. Our films are grown on polycrystalline nickel (Ni) foils by a CVD-based non-equilibrium surface segregation process, as described in detail previously<sup>7</sup>. The films have generally non-uniform thickness at large scale (containing regions as thin as  $\sim 2$  graphene layers and as thick as tens of layers), yet may still have good electronic properties for device applications as described here. Following the growth, the Ni substrate is etched off in acid (Fig. 1) and the graphene film is transferred to a Si/SiO<sub>2</sub> substrate (Fig. 2). The typical size of as-grown films ranges from mm to cm and is mainly limited by the size of the CVD chamber. After the transfer, the film is lithographically patterned into GFET devices, with deposited Cr/Au as source and drain electrodes. The doped Si serves as the back gate (Fig. 3). Fig. 4 shows a representative large-sized GFET, fabricated with optical lithography and patterned as a Hall bar. Typical ambipolar field effects measured in a similar large device (“A”) are shown in Fig. 5 (4-terminal resistance vs gate voltage,  $V_{\text{gate}}$ ; measurements are performed at low temperature to access a large  $V_{\text{gate}}$  range without gate leakage). Effective mobilities for electrons and holes extracted from the field effect<sup>3</sup> reach  $\sim 2000$  cm<sup>2</sup>/Vs (away from the “charge-neutral point” peak in  $R$  vs  $V_{\text{gate}}$ ). Hall effects (Fig. 6) confirm the ambipolar nature (majority carrier type switching from p- to n-) of the FET. On a smaller-sized GFET (Fig. 7, patterned in van der Paw geometry) fabricated by e-beam lithography (EBL), we observe ambipolar field effect (plotted as calculated conductivity vs  $V_{\text{gate}}$ ) with even higher mobilities ( $\sim 4000$ - $6000$  cm<sup>2</sup>/Vs). Back-gated ambipolar GFET devices with comparable mobilities  $\sim 2000$ - $4000$  cm<sup>2</sup>/Vs have also been recently fabricated with few-layer graphitic films grown by CVD on deposited Ni thin films<sup>8,9</sup>. Being flexible, transparent, easily transferrable to nearly any substrates<sup>9</sup> and producible in a scalable manner, CVD-grown few-layer graphitic films can enable a wide range of electronic applications.

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<sup>1</sup>K. S. Novoselov *et al.*, Science 306, 666 (2004); <sup>2</sup>C. Berger *et al.*, Science 312, 1191 (2006); <sup>3</sup>Y.Q.Wu *et al.*, APL 92, 092102 (2008); <sup>4</sup>I.Meric *et al.*, Nature Nano. 3, 654 (2008); <sup>5</sup>Y.M.Lin *et al.*, Nano Lett. 9, 254 (2009); <sup>6</sup>C. Oshima and A. Nagashima, J. Phys. C 9, 1 (1997); <sup>7</sup>Q.Yu *et al.*, APL 93, 113101 (2008); <sup>8</sup>A.Reina *et al.*, Nano Lett. 9, 30 (2009); <sup>9</sup>K.S. Kim *et al.*, Nature 457, 706 (2009).

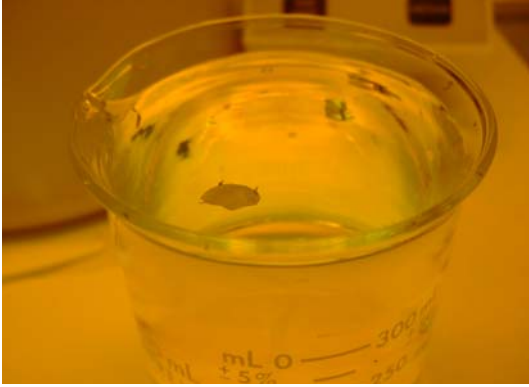


Fig. 1. A CVD-grown graphitic film etched from Ni by  $\text{HNO}_3$ . A relatively thick and readily visible film is shown here. Thinner films can be almost transparent.

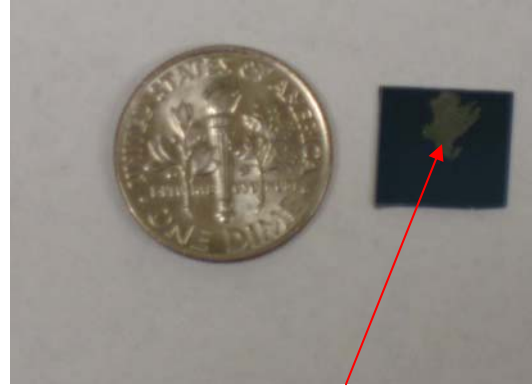


Fig. 2. A CVD-grown graphitic film transferred to Si/SiO<sub>2</sub> wafer (doped Si covered by 300nm SiO<sub>2</sub>), placed next to a dime.



Fig. 3. Schematic cross section of the GFET device made from CVD grown graphitic film transferred to Si/SiO<sub>2</sub>.

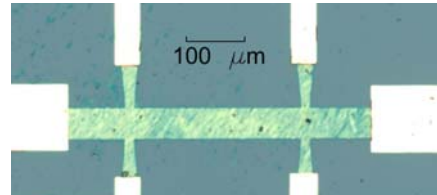


Fig. 4. Optical microscope image (top view) of a large-size GFET device patterned into a Hall bar.

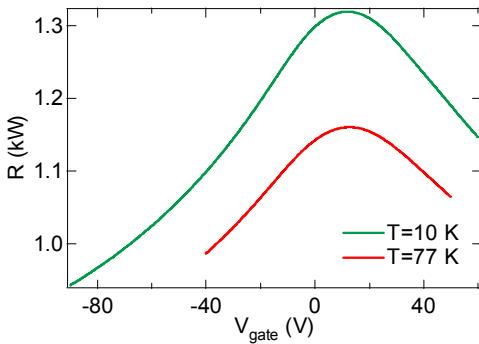


Fig. 5. Ambipolar field effect (resistance) of a large-size GFET device ("A"), with electron and hole mobilities reaching  $\sim 2000 \text{ cm}^2/\text{Vs}$ .

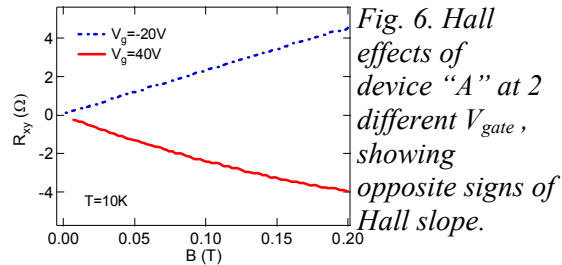


Fig. 6. Hall effects of device "A" at 2 different  $V_{gate}$ , showing opposite signs of Hall slope.

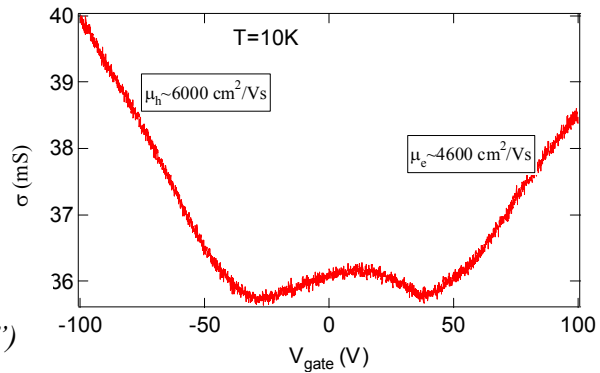


Fig. 8. Ambipolar field effect (conductivity) of device "B", with mobilities reaching  $\sim 4000\text{-}6000 \text{ cm}^2/\text{Vs}$ .



Fig. 7. A small GFET device ("B") made by EBL (scale bar =  $34.6 \mu\text{m}$ ). Black lines on film are wrinkles.