ELECTRONIC PROPERTIES OF Au NANOCLUSTERS/SEMICONDUCTOR STRUCTURES WITH LOW RESISTANCE INTERFACES

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This thesis is dedicated to my wife Kwihyun Nam, our families, and to the memory of my father.

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ABSTRACT

Takhee Lee. Ph.D., Purdue University, May, 2000. Electronic Properties of Au Nanoclusters/Semiconductor Structures with Low Resistance Interfaces.
Major Professor: Ronald G. Reifenberger.

Self-assembled metal/molecule/semiconductor nanostructures are utilized to define nanoelectronic device contact structures and are characterized using ultra high vacuum (UHV) scanning tunneling microscopy (STM).

As examples of the controlled nanostructures for nanoelectronic device applications, nonalloyed ohmic contact nanostructures have been utilized on a surface layer of LTG:GaAs, i.e., GaAs grown at a low temperature by molecular beam epitaxy. The controlled-geometry nanocontact is obtained by depositing a 4 nm diameter single crystal Au cluster (truncated octahedral shape) onto n-GaAs(100) having LTG:GaAs based ohmic contact layers using *ex-situ* chemical self-assembly techniques. A self-assembled monolayer (SAM) of xylyl dithiol ($HS-CH_2-C_6H_4-CH_2-SH$) is formed on LTG:GaAs and provides an effective organic metal/semiconductor interface having both a robust mechanical tethering and a strong electronic coupling between the Au nanoclusters and the LTG:GaAs surface.

UHV STM is used to locate and probe the electronic properties of the nanocontacts. STM current versus voltage (I-V) data measured over Au nanoclusters exhibit an ohmic behavior with a significant enhancement in the conduction for low bias voltages compared to I-V data over the SAM-coated LTG:GaAs substrate. A specific contact resistance of 10^{-6} - 10^{-7} $\Omega \cdot \mathrm{cm}^2$ and a current density of 10^6 - 10^7 A/cm^2 have been measured on the nanocontacts from STM. The ohmic nanocontact is mainly due to the sequential tunneling through the xylyl dithiol layer and the LTG:GaAs layer while a midgap band of defect states in the LTG:GaAs layer assists conduction as if it effectively reduces the barrier width.

Another interesting approach is to combine the nanoscale elements (Au clusters) and ordering from self-assembly processes with a procedure which can impose an arbitrary larger-scale pattern to form the specific configurations and interconnections needed for computation. Toward this goal, high-quality hexagonal close-packed arrays of Au nanoclusters (5 nm in diameter) are formed within patterned regions on active GaAs substrates having LTG:GaAs cap layer and are characterized using STM. This approach utilizes a patterned template which guides Au nanoclusters into pre-selected regions with xylyl dithiol. The directed self-assembly techniques used to fabricate these structures have the potential to provide high-throughput fabrication of nanostructures for nanoelectronics and other nanoscale applications.

1. INTRODUCTION

Since the first successful single transistor was built, device fabrication technology has grown at a tremendous rate and device size is getting smaller and smaller. The number of transistors and capacitors in an integrated circuit has been doubled about every 18 months.[1,2] Nowadays, 1-gigabit (Gb) dynamic random access memory (DRAM) which has more than 100,000,000 device components such as transistors and capacitors is currently being produced on thumbnail-sized Si chip.

With further downscaling of semiconductor devices, there will be a transition from the present fabrication technology in micrometer length scale to the new technology in nanometer length scale, so called nanotechnology.[3,4] This nanotechnology requires a clear understanding of physical properties of nanometer scale systems. Example phenomena or devices at this scale are such as Coulomb blockade and staircases,[5,6] single electron tunneling devices,[7,8] and quantum-based electronic devices.[9]

The ability to fabricate nanometer scale structures are essential in nanotechnology. Direct use of conventional lithographic techniques such as electron beam lithography[10,11] or scanning probe microscope-related nanolithography[12,13] become expensive and slow when used to define nanoscale features. Self-assembly techniques provide a means to realize nanostructures such as quantum dots and other electronic/optoelectronic device configurations. Because these techniques do not rely on lithography to realize the specific nanostructures and assemblies, they can represent efficient, high throughput fabrication approaches. There are two classes of self-assembly which have attracted interest for electronic devices and materials applications.

The first class involves the formation of semiconductor quantum dots either through controlled growth techniques such as the Stranski-Krastanow (S-K) growth technique[14–16] or by deposition of semiconductor materials into regular arrays of pores in an insulating matrix.[17] This approach provides an interesting material, namely arrays of quantum dots, but typically does not lend itself to the assembly of specific device structures or interconnected devices. For self-assembled semiconductor structures, the electronic device functionality has been limited by the difficulty in achieving suitable interfaces for passivating and contacting the resulting islands or dots.

A second class of self-assembly approaches involves the formation of semiconductor or metal nanoclusters and 2-D or 3-D assemblies of these clusters.[18–26] Some of these self-assembled structures have potential applications as electronic materials, such as uniform arrays of clusters in which the cluster-to-cluster resistance can be controlled by the choice of intercluster linking molecule.[18] In addition, room-temperature Coulomb blockade has been realized in self-assembled metal/molecular nanostructures.[5] However, to date structures based on metal or semiconductor clusters have not provided the types of functionalities provided by semiconductor devices.

In this study, a self-assembly approach of metal/molecule/semiconductor nanostructures is utilized to define nanoelectronic device and contact structures. The overall goal of this approach is to combine the nanostructures that can be realized with self-assembly with the robust functionality provided by semiconductor device structures (gain, directionality, etc.) to utilize functional nanoelectronic devices and contact applications. The resulting structures have well controlled dimensions and geometries provided by the chemical self-assembly and have stable, low-resistance interfaces realized by the chemically stable semiconductor cap layers and additional passivation provided by organic tether molecules.

As examples of the high quality interfaces and controlled nanoscale structures for nanoelectronic device applications, nonalloyed ohmic contact nanostructures have been utilized on a surface layer of LTG:GaAs,[27,28] i.e., GaAs grown at a low temperature by molecular beam epitaxy as a chemically stable semiconductor surface. In contrast to typical *ex-situ* ohmic contacts formed on n-type semiconductors such as GaAs, this approach can provide uniform contact interfaces which are essentially planar injectors, making them suitable as contacts to shallow devices with overall dimensions below 50 nm. The controlled-geometry nanocontact is obtained by depositing a 4 nm diameter single crystalline Au cluster (truncated octahedral shape) onto the LTG:GaAs based ohmic contact layers using *ex-situ* chemical self-assembly techniques. A self-assembled monolayer (SAM)[29] of xylyl dithiol (HS-CH_2-C_6H_4-CH_2-SH) is employed on LTG:GaAs. This molecular layer forms an effective organic metal/semiconductor interface and provides both a robust mechanical tethering and a strong electronic coupling between the Au nanoclusters and the LTG:GaAs surface. Ohmic nanocontacts are fabricated on n-GaAs(100) having undoped LTG:GaAs (n-type) and Be-doped LTG:GaAs (still n-type) cap layers. A ultra high vacuum (UHV) scanning tunneling microscopy (STM) is used to locate and probe the electronic properties of the nanocontacts. STM current versus voltage (I-V) data measured over Au nanoclusters exhibit an ohmic behavior with a significant enhancement in the conduction for low bias voltages compared to I-V data over the SAM-coated LTG:GaAs substrate, regardless of the dopant type of LTG:GaAs cap layer. When an undoped LTG:GaAs cap layer is used for ohmic nanocontacts, a specific contact resistance of $\sim 1 \times 10^{-6}$ Ω·cm^2 and a current density of $\sim 1 \times 10^{6}$ A/cm^2 have been measured from STM. For the case of nanocontacts on a Be-doped LTG:GaAs cap layer, the corresponding values are $\sim 1 \times 10^{-7}$ Ω·cm^2 and $\sim 1 \times 10^{7}$ A/cm^2, respectively. The ohmic nanocontact is mainly due to the tunneling from Au cluster into GaAs layers while a midgap band of defect states (midgap states) in the LTG:GaAs layer assists conduction as if it effectively reduces the barrier width. Improved surface stability as evidenced by a lower oxidation rate and conduction through the large amount of the midgap states distributed around the Fermi level in Be-doped LTG:GaAs provide a natural explanation for the higher quality ohmic contact properties of the nanocontact to the Be-doped LTG:GaAs cap layer.

In order to realize devices and/or circuits with functionalities comparable to conventional integrated circuits, it will be necessary to break the symmetry of the uniform self-assembled networks in controlled ways, i.e., to impose patterns to provide gain, non-uniform interconnect structures and directionality. An interesting approach would be to combine the nanoscale elements (Au nanoclusters) and ordering from self-assembly processes with a procedure which can impose a somewhat arbitrary larger-scale pattern to form the specific configurations and interconnections needed for computation. In anticipation of these possibilities, architectural configurations using a hybrid self-assembly/semiconductor device approach have been described and could be realized using cells consisting of 2-D networks of nanoscale metallic nodes on active semiconductor mesas with well-defined local intercell connections.[30]

Toward this goal, high-quality hexagonal close-packed arrays of Au nanoclusters ($\sim$ 5 nm in diameter) are formed within patterned regions on active GaAs substrates employing LTG:GaAs cap layer and are characterized using STM. The approach utilizes a patterned template which guides the self-assembled elements (Au nanoclusters) into pre-selected regions with a molecular tether (xylyl dithiol). The local ordering at the nanometer scale is provided by a chemically driven self-assembly process, while the arbitrary global pattern is defined by the patterned template with a soft lithographic technique. The directed self-assembly techniques used to fabricate these nanostructures have the potential to provide high-throughput fabrication of structures for nanoelectronics applications.

In this thesis, a review of STM and STM spectroscopy are presented in chapter 2 and 3, and STM instrumentation is discussed in chapter 4. As examples of self-assembled nanostructures for nanoelectronic application, nonalloyed ohmic contact to n-GaAs(100) at the nanometer scale is discussed in chapter 5 and 6, and the ohmic contact mechanism is discussed in chapter 7. Fabrication and characterization of patterned self-assembled arrays of Au nanoclusters are presented in chapter 8.

2. SCANNING TUNNELING MICROSCOPY

2.1 Introduction

The experimental techniques to characterize nanometer scale systems require both a direct imaging and characterization at the nanometer scale. High resolution microscopic techniques, such as scanning electron microscopy (SEM), transmission electron microscopy (TEM), scanning tunneling microscopy (STM)[31,32] and atomic force microscopy (AFM) can be used to obtain direct images of the material surface at the nanometer scale. Some other surface analytical techniques, such as X-ray photoemission spectroscopy (XPS), ultraviolet photoemission spectroscopy (UPS), X-ray diffraction and low-energy electron diffraction (LEED) can only provide spatially averaged information. Among these techniques, STM and STM-based spectroscopic techniques can provide a proper experimental tool for both imaging and characterization.

STM was invented in early 1980's by Binnig and Rohrer and is a powerful technique to image the real space of a surface structure.[33] STM and STM-related techniques are widely used in the areas of physics, chemistry, material science, biology, etc. At the early stage of STM, the main application of STM was to image a material surface. Nowadays, STM is used to study the electrical properties of a material and even to modify the surface at the atomic scale.[34,35] Recently, STM has been used to manipulate the bonding of a carbon monoxide molecule.[36] Therefore, STM has become an important technique in surface science as the size of a device decreases to the nanometer scale.

2.2 Principle of STM Operation

STM images can be obtained by probing a tip over the surface of a sample as shown in Fig. 2.1. When a sharp metal tip is brought very close to a sample (typically a few nanometers above the sample), the wave functions of tip and sample overlap and electrons will tunnel through the potential barrier between the surfaces when a bias voltage is applied. The vacuum gap between two conducting electrodes, in this case the tip and sample, plays the role as a barrier. The solution of Schrödinger's equation for one dimensional rectangular barrier problem has the form of

$$\psi \propto e^{-\kappa z} \quad . \tag{2.1}$$

Therefore, for small voltages, the resulting tunneling current I decays exponentially with barrier width as[37]

$$I \propto e^{-2\kappa z} \quad , \tag{2.2}$$

where z is the gap distance between tip and sample and κ is called decay constant which is related to the local work functions ϕ of tip and sample as[37]

$$\kappa = \hbar^{-1}\sqrt{2m\phi} \quad , \tag{2.3}$$

where m is the mass of electron.

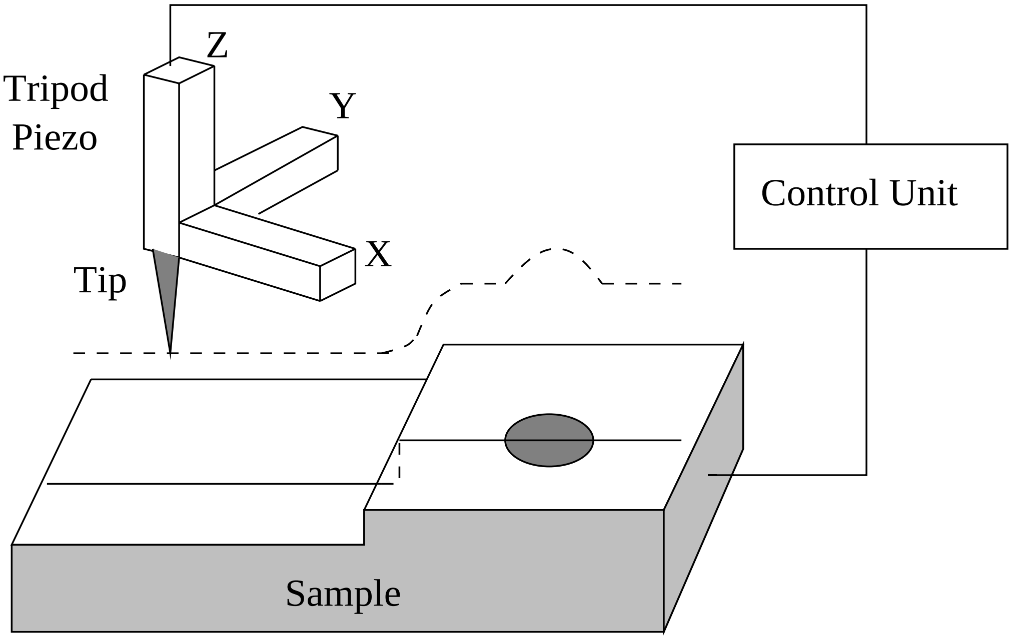


Figure 2.1

Principle of STM operation. The x and y piezoelectric scanners scan over the surface while the control unit applies a proper voltage to the z piezoelectric scanner. The broken line indicates the vertical displacement in a scan over a surface step and a surface inhomogeneity.

For tunneling between two electrodes with an applied bias V as shown in Fig. 2.2, only the states within eV of the Fermi energy can tunnel. Other states can't tunnel because of the exclusion principle. For energies above the Fermi level of the negative electrode (tip in case of Fig. 2.2), there are no filled electron states on either side. For energies below the Fermi level of the positive electrode (sample), there are no empty states for an electron to tunnel into either side. Actually, the transmission probability is largest for the electrons near the Fermi level, therefore STM relies on the tunneling current carried by energy states near the Fermi level.

Work functions of most materials are around 4-5 eV, κ is thus typically 1 Å^{-1}. This implies that for 0.1 nm change in the tip sample separation, an order of magnitude change in current will result. This explains the basic principle of STM operation in obtaining atomic resolution. Of course, since the tip has a finite radius, the surface topography is determined with a finite lateral resolution. Typically, on atomically flat surfaces, STM has a vertical resolution of 0.01 nm and a lateral resolution of 0.1 nm.

Achieving such atomic resolution images requires a precise control of the tip position and vibration isolation to less than 0.1 nm. The precise control of the tip position in atomic range can be obtained with a piezoelectric material which has a property of undergoing a small dimensional change when an electric voltage is applied. Also several ways are used for the vibration isolation, such as a double stage spring suspension with magnetic eddy-current damping system and an isolation setup of the STM chambers from the floor and ceiling.

2.3 Experimental Modes

The STM can be operated in either the constant current mode or the constant height mode, as shown in Fig. 2.3.

In the constant current mode of operation [Fig. 2.3 (a)], the tip is scanned across the surface with the tip sample separation kept constant. Since the tunneling current is dependent on the tip sample separation, this separation is kept constant by changing the voltage applied to the z piezoelectric scanner using a feedback circuit. The correction voltage δV_z applied to the z piezoelectric scanner is recorded and is displayed while the tip scans over the surface. In this mode, the scan rate can not be very fast because of the limited range of the feedback circuit. The height of surface features can be derived from the correction voltage δV_z and the sensitivity of the z piezoelectric scanner α in the following simple form:

$$\delta z = \alpha \times \delta V_z \quad . \tag{2.4}$$

For the STM system used in this study, the sensitivities are 1.4 nm/V for x and y piezoelectric scanners and 1.6 nm/V for z piezoelectric scanner.

In the constant height mode [Fig. 2.3 (b)], the tip is scanned rapidly across the surface at a constant height while the tunneling current is recorded. This is faster than the constant current mode since the tip requires no z adjustment (feedback) during the scan. The exact topographic height is not easily calculated because a separate determination of work function ϕ is required in this mode.

2.4 Spectroscopy

Beside the topographic modes of operation, further information can be obtained from STM by using spectroscopic modes of operation where the voltage dependence of the tunneling current is studied. This is known as scanning tunneling spectroscopy (STS). Since STM relies on the tunneling current carried by energy states near the Fermi level, for example, current-voltage (I-V) measurement can provide information about the electronic structure of the sample by probing the sample density of states (DOS) as a function of energy relative to the Fermi level of the sample. The polarity of the applied voltage bias determines whether electrons tunnel into the unoccupied of the sample (positive sample bias) or out of the occupied states (negative sample bias).

Another useful method of obtaining spectroscopic information is measuring a full I-V curve at each pixel of a topographic image simultaneously. This is called current imaging tunneling spectroscopy (CITS). CITS is a very useful spectroscopic method because CITS data can reveal the electrical property of a certain region in a topographic image.

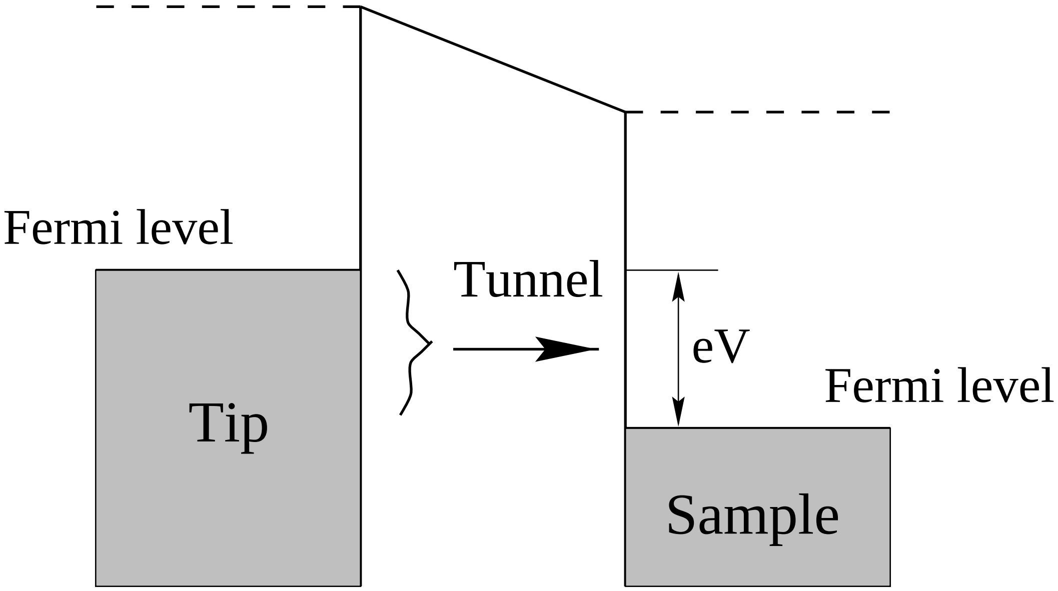


Figure 2.2

Energy level diagram of tip and sample with an applied bias V. The tip is negatively biased in this case, so that the energy level of the tip is shifted upward.

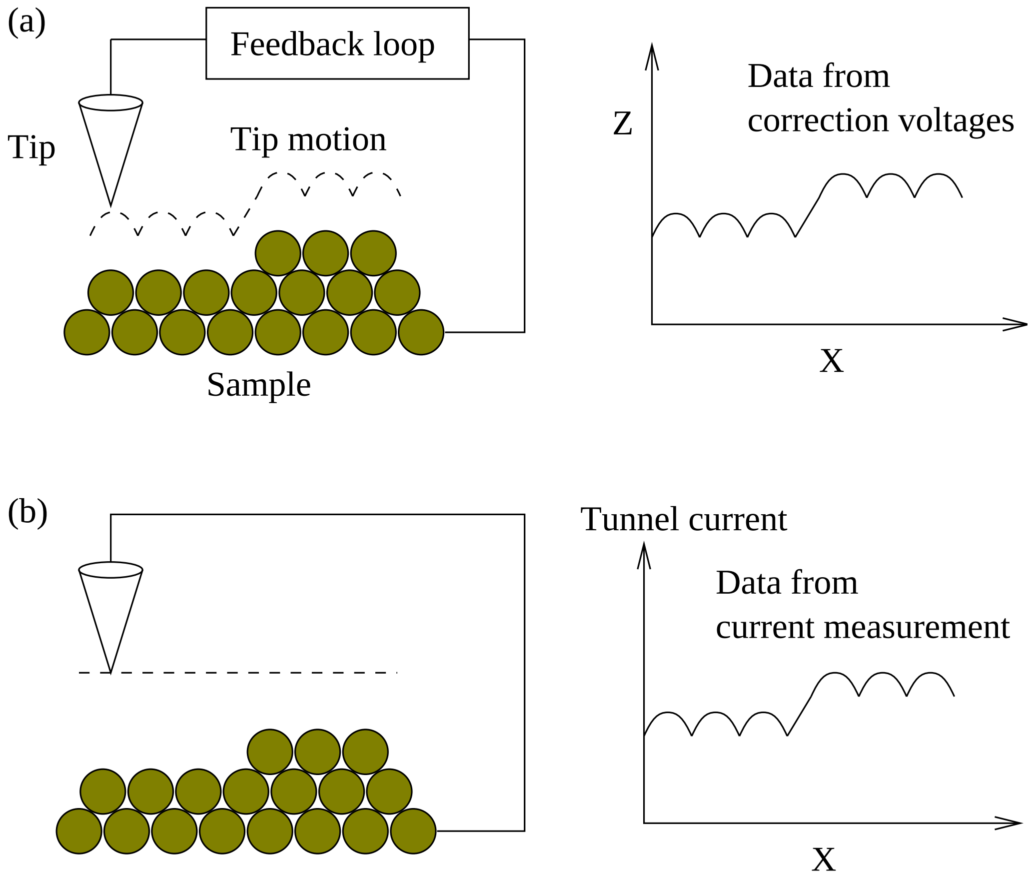


Figure 2.3

Schematics of two modes of STM operation. In constant current mode (a), the feedback loop keeps the tunnel current constant and the correction voltages are recorded as the data. In constant height mode (b), the tip is scanned over the sample without feedback loop and the tunnel current values are recorded as the data.

3. SCANNING TUNNELING SPECTROSCOPY

3.1 Tunneling Current Theory

The tunneling current between two metallic electrodes, tip and sample, can be written by Fermi Golden rule of the first order perturbation theory as follows.[38]

$$I(V) = \frac{2\pi e}{\hbar} \sum_{t,s} (f(E_s)[1 - f(E_t - eV)] - f(E_t - eV)[1 - f(E_s)])|M_{t,s}|^2 \delta(E_t - E_s) \ . \tag{3.1}$$

In this equation, V is the applied voltage to the sample, $f(E)$ is the Fermi-Dirac distribution function, E_t and E_s are the energies of the state of tip and sample relative to the Fermi level of each surface, and $M_{t,s}$ is the matrix element between the state ψ_t of the tip and the state ψ_s of the sample in the absence of tunneling as given by Bardeen's model,[39]

$$M_{t,s} = \frac{\hbar}{2m} \int (\psi_t^* \nabla \psi_s - \psi_s^* \nabla \psi_t) \cdot d\mathbf{S} \ \ , \tag{3.2}$$

where the integral is over the any surface lying entirely within the barrier region.

Under the assumptions that (i) the tip has uniform density of states, (ii) only s-wave tip wave function is important, (iii) the unperturbed wave functions of tip and sample can be used when the tip sample interactions are weak, and (iv) the bias voltage is low (< 10 mV), Tersoff and Hamann predicted that the tunneling current is proportional to the local density of states (LDOS) of the sample.[38]

The low bias approximation is often violated since many STS experiments are conducted at more than 1 V. Using WKB approximation, the tunneling current can be expressed as

$$I = \int_{-\infty}^{\infty} [f(-eV+E) - f(E)]\, \rho_s(r,E)\, \rho_t(r,-eV+E)\, T(E,eV,z)\, dE \ , \tag{3.3}$$

where $\rho_s(r,E)$ and $\rho_t(r,-eV+E)$ are the density of states (DOS) of the sample and tip at location r and energy E measured with respect to their individual Fermi levels. For negative sample bias, $eV < 0$ and for positive sample bias, $eV > 0$. The transmission probability function $T(E,eV,z)$ for electrons with energy E, applied bias voltage V, and tip to sample distance z is given in the WKB approximation as

$$T(E,eV,z) = \exp\left[-\frac{2z\sqrt{2m}}{\hbar} \sqrt{\frac{\phi_t + \phi_s}{2} + \frac{eV}{2} - E} \right] \ , \tag{3.4}$$

where ϕ_t and ϕ_s are the work functions of tip and sample. [$T(E,eV,z)$ will be a function of position r of sample and tip when ϕ_t and ϕ_s have local variation.] In the limit of low surface temperature ($k_B T << eV$), the tunneling current is then,

$$I = \int_{0}^{eV} \rho_s(r,E)\, \rho_t(r,-eV+E)\, T(E,eV,z)\, dE \ . \tag{3.5}$$

If $eV < 0$ (negative sample bias), the transmission probability function is largest for $E = 0$ corresponding to electrons at the Fermi level of the sample, and if $eV > 0$ (positive sample bias), the transmission probability function is largest for $E = eV$ corresponding to electrons at the Fermi level of the tip. Therefore, the tunneling probability is always largest for electrons at the Fermi level of whichever electrode is negatively biased. Fig. 3.1 (a) shows a transmission probability as a function of energy using $\phi_t = \phi_s = 4.0$ eV, $z = 1.0$ nm, and the applied sample bias $V =$ 2.0 V. In this case, the transmission probability is largest at the Fermi level of tip indicated by $E = eV = 2.0$ eV, as shown in Fig. 3.1 (b).

Fig. 3.2 is an energy level diagram illustrating the effect of the bias voltage polarity. If the tip and sample is close to each other, the Fermi levels of the tip and sample will be in the equilibrium with no bias [Fig. 3.2 (a)]. At a negative sample bias (a positive bias is applied to the tip while the sample is grounded), the energy level of the sample will shift upward, as in Fig. 3.2 (b). In this case, electrons will tunnel from the occupied states of the sample into the unoccupied states of the tip. At a positive sample bias, the energy level of the tip will shift upward as in Fig. 3.2 (c) and the electrons will tunnel from the occupied states of the tip into the unoccupied states of the sample. Therefore, the STM tip follows the contour of occupied states of sample at negative sample bias, while it follows the contour of unoccupied states of sample at positive sample bias. Some application of this voltage-dependent imaging were made with Si(111)-7 × 7,[40] Si(111)-2 × 1,[41] InP(110),[42] and GaAs(110).[43]

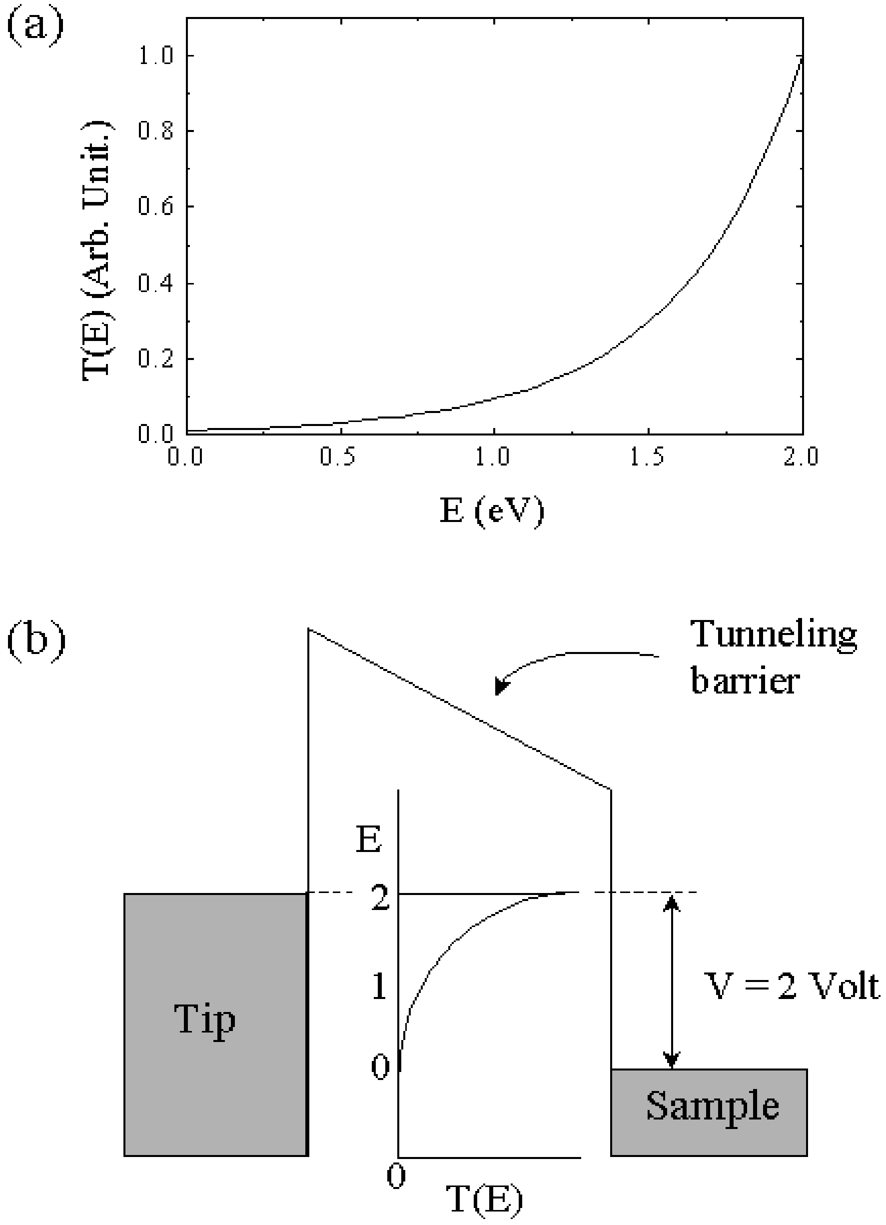


Figure 3.1

(a) A transmission probability as a function of energy using $\phi_t = \phi_s = 4.0$ eV, $z =$ 1.0 nm, and an applied sample bias $V = 2.0$ V. (b) The transmission probability is largest at the Fermi level of tip indicated by energy $E = eV = 2.0$ eV.

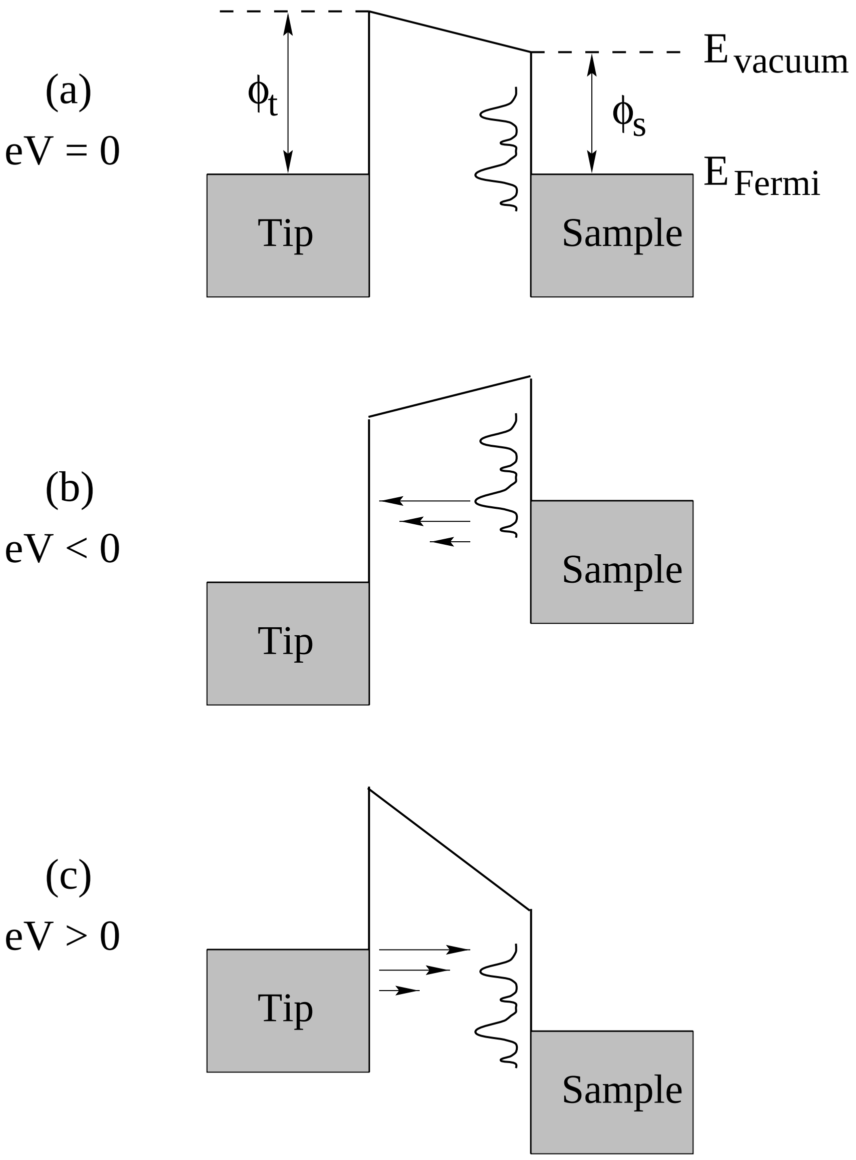


Figure 3.2

Energy level diagram of tip and sample: (a) Tip and sample are in thermal equilibrium with no bias; (b) negative sample bias; (c) positive sample bias. ϕ_t and ϕ_s are the work functions of the tip and sample, respectively.

3.2 *I*-*V* Characteristics

The first derivative of the tunneling current with respect to applied voltage (dI/dV, differential conductivity) can be written as

$$\frac{dI}{dV} = \rho_s(r,eV)\rho_t(r,0)T(eV,eV,z) + \int_0^{eV} \rho_s(r,E)\rho_t(r,E-eV)\frac{dT(E,eV,z)}{dV}dE \ , \tag{3.6}$$

where the tip is considered to be a metal with a constant density of states or at least a slowly varying density of states implying that $d\rho_t(-eV+E)/dV \approx 0$. The first term in this equation is the product of the density of states of the sample, the density of states of the tip, and the tunneling transmission probability T. The second term reflects the voltage dependence of the tunneling transmission probability. Since T is a smooth monotonically increasing function of the applied voltage V, dI/dV can provide a measure of the density of states as a function of energy at any particular location on the surface of the sample.

Dividing both sides of differential conductivity dI/dV by the ratio I/V, and then dividing both by the factor $T(eV,eV)$ gives

$$\frac{dI/dV}{I/V} = \frac{\rho_s(eV)\rho_t(0) + \int_0^{eV}\left[\frac{\rho_s(E)\rho_t(E-eV)}{T(eV,eV)}\right]\left[\frac{dT(E,eV)}{dV}\right]dE}{\frac{1}{eV}\int \rho_s(E)\rho_t(E-eV)\left[\frac{T(E,eV)}{T(eV,eV)}\right]} \ . \tag{3.7}$$

Feenstra, et al. showed that since $T(eV,eV)$ and $T(E,eV)$ appear as ratios in the second term in the numerator and in the denominator, their dependence on the tip sample separation and the applied voltage tends to cancel.[44] This normalized conductivity $(dI/dV)/(I/V)$ is simply

$$\frac{dI/dV}{I/V} = \frac{d(logI)}{d(logV)} = \frac{\rho_s(eV)\rho_t(0) + A(V)}{B(V)} \ . \tag{3.8}$$

Assuming that $A(V)$ and $B(V)$ vary slowly with voltage, this provides a measure of density of states of the surface of the sample.

$$\frac{dI/dV}{I/V} \sim \rho_s(V) \ . \tag{3.9}$$

Fig. 3.3 is an example of a normalized conductivity calculated numerically using I-V raw data measured on a GaAs grown at a low temperature (LTG:GaAs). Near the band edges at -0.6 eV and 0.5 eV, the normalized conductivity tends to diverge simply because both the tunnel current and conductivity approach zero at the band edge. Therefore, I/V is no longer a valid estimator of the tunneling transmission term. One method to eliminate the divergence in the normalized conductivity is to broaden the function I/V by convolution of a suitable function, thereby eliminating the false zeros of I/V within the bandgap.[45] An example of the broadening of normalized conductivity using the same I-V raw data is shown in Fig. 3.4. For ease of computation the convolution is Fourier transformed, in this case it is corresponding to a low pass filter of the form $2/(1+exp[f/f_{cutoff}])$ where f is the frequency component of the voltage.

A schematic illustrating the I-V measurement is shown in Fig. 3.5. A region of interest is first centered in the STM image before the scan size is set to zero. When the scan size is not zero, I-V measurement is performed in the middle of each scan line. After the tip sample separation is adjusted by the feedback system with a set voltage V_{set} and a set current I_{set} for 2 msec, the tip position is kept fixed while the bias voltage is swept from a start voltage V_1 to a final voltage V_2 and

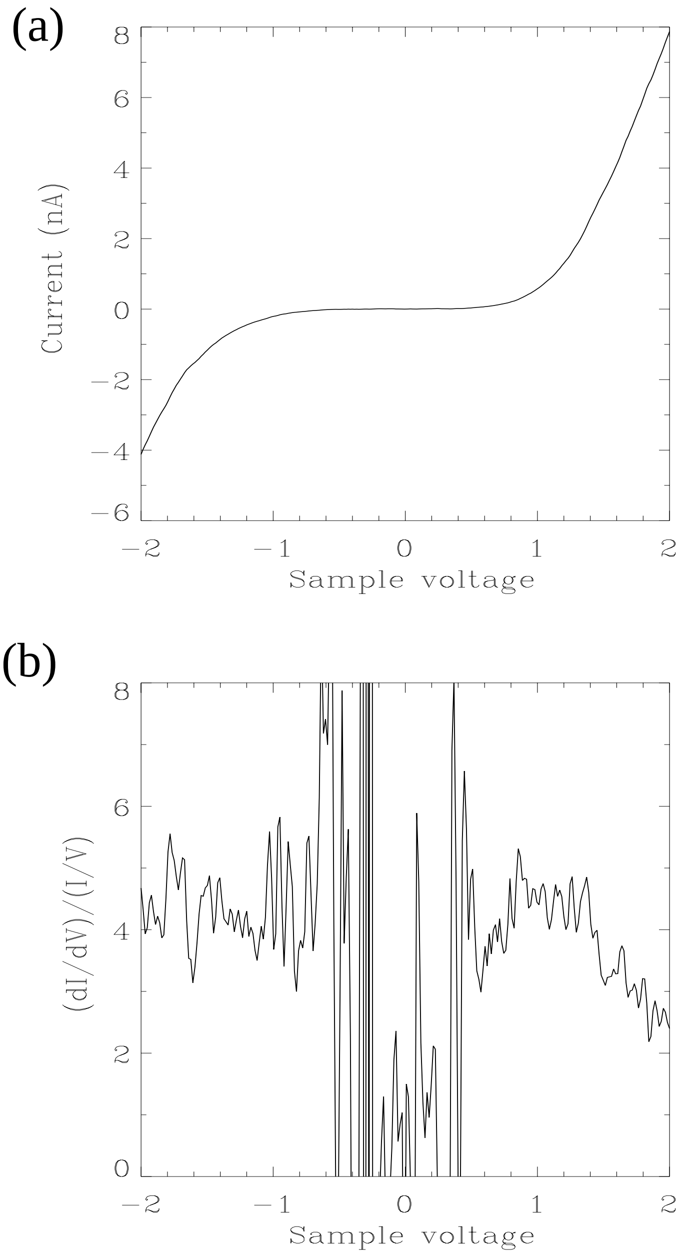


Figure 3.3

(a) *I*-*V* data measured on LTG:GaAs. (b) Normalized conductivity $(dI/dV)/(I/V)$ calculated numerically using the *I*-*V* data. Normalized conductivity is extremely noisy at the band edge because both the tunnel current and conductivity approach zero and the ratio diverges.

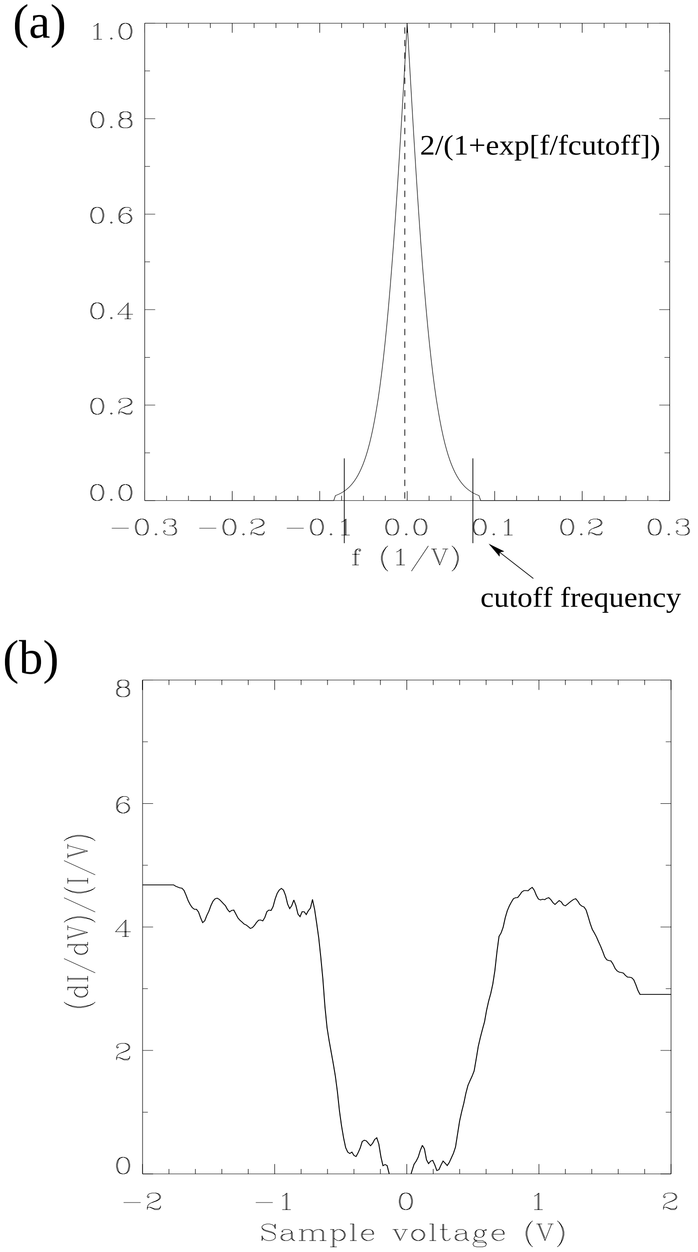


Figure 3.4

(a) Convolution filter function in Fourier transformed space. (b) Normalized conductivity calculated with broadening and filtering using the low pass filter function.

the resulting tunneling current is measured. The tip sample separation is adjusted again by the feedback with the set conditions to minimize thermal drift of the z piezoelectric scanner and then the process is repeated. Since a single I-V sweep is noisy, averaging I-V data is required. Typical time duration for a single I-V sweep is 40 msec. This time duration depends on two parameters, sampling delay and number of data points. The sampling delay is the number of measurement of current at each bias voltage. Typical sampling delay is 3, that is, three times measurements of current are performed and averaged as the current data at each bias voltage. The number of data points of I-V is selected among 128, 256, and 516. Typical number of data point is 256.

3.3 Current Imaging Tunneling Spectroscopy

The full advantage of STM operation is a spectroscopic measurement simultaneously with a topographic image. This technique is called current imaging tunneling spectroscopy (CITS).[46] Fig. 3.6 illustrates the CITS measurement technique. The tip's z position is measured first at a pixel of an image which has typically 128 × 128 pixels. Then, the feedback circuit is opened and the tip position is held fixed while the bias voltage is ramped and the tunneling current is measured at 44 bias voltages. The tip is moved to the next pixel of the topographic image and the process is repeated. Thus, one can create a topographic image and 44 tunneling current images at different voltages.

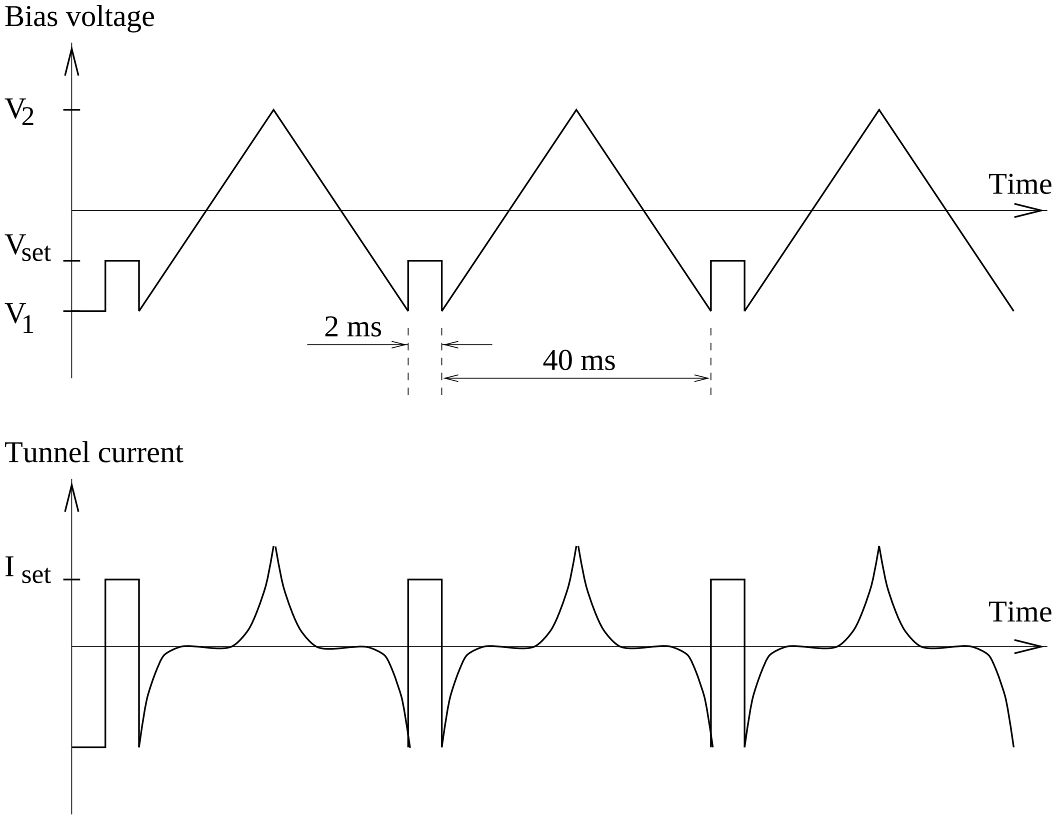


Figure 3.5

A schematic illustrating averaging technique to perform *I*-*V* measurement.

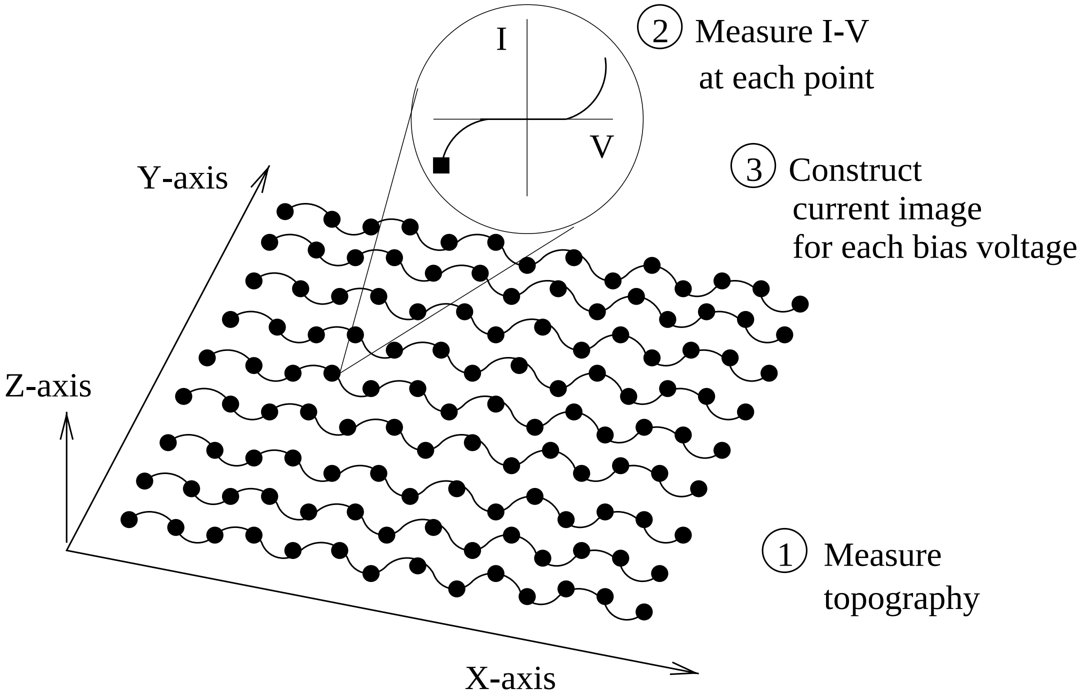


Figure 3.6

A schematic illustrating the current imaging tunneling spectroscopy (CITS) technique. The square point in I-V represents a tunneling current measured at V_{set} which is used to obtain a topographic image.

Fig. 3.7 is a CITS image obtained on 4 nm diameter Au clusters on an organic molecule (xylyl dithiol) coated LTG:GaAs. The center image is the topographic image and there are 44 current images at different voltages from -2 V to 2 V. The bright regions in the topographic image are the Au clusters and there are also corresponding bright regions in the current images. Bright region in the topographic image represents higher region compared with a dark region. Similarly, bright region in the current images represents higher current or higher conductivity region. Therefore, one interesting result from this CITS image is the enhancement of conductivity over the Au clusters, which will be explained in detail in chapter 6 and 7.

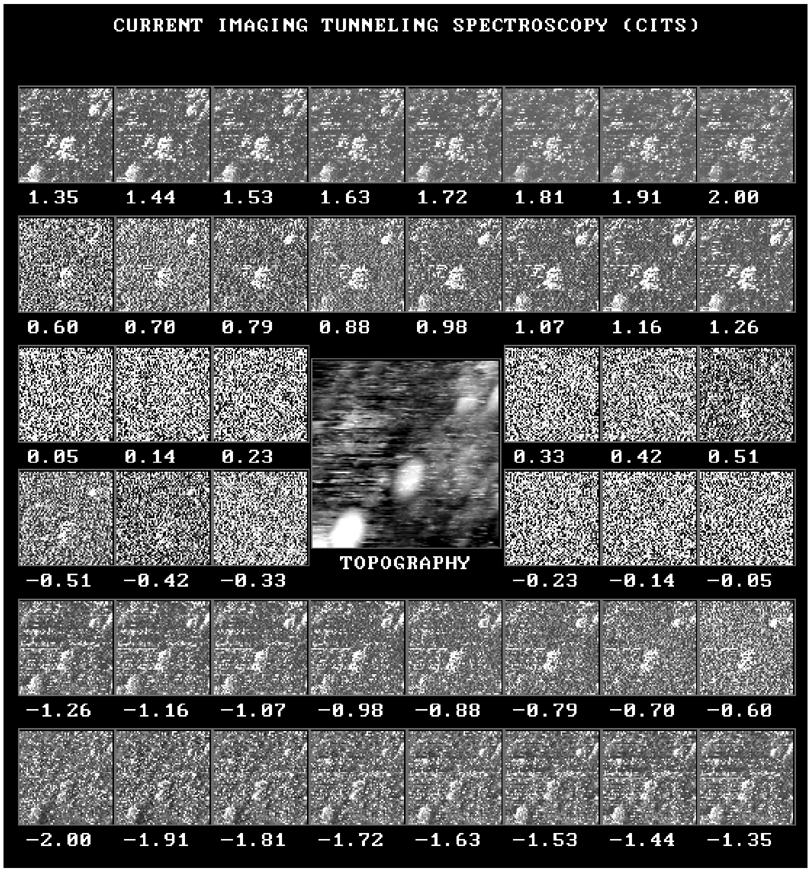


Figure 3.7

A 70 nm × 70 nm CITS image of 4 nm diameter Au clusters tethered on xylyl dithiol coated LTG:GaAs, acquired with a set current I_{set} of 0.6 nA, a set sample voltage V_{set} of -2.0 V, and a scan rate of 4 Hz. The circular bright regions represent Au clusters both in the topographic image and in the current images at different bias voltages.

4. STM INSTRUMENTATION

4.1 UHV STM System (Vibration Isolation UHV STM System)

The frame of any STM instrument is subject to mechanical vibrations transmitted from the floor or the walls. For normal operation of STM, the tip is typically a few nanometers above the sample. Therefore even the smallest vibrations, such as those caused by sound in air and by people working around the building, can affect the STM experiment. Fig. 4.1 is a schematic of the vibration isolated STM system used in this study. The entire chamber is hung with bungee cables during the experiment to isolate the mechanical vibration from the floor and the ceiling. This hanging method is not enough to isolate the very small vibration, so that a double stage spring suspension system with magnetic eddy-current damping system is used in the STM head, as shown in Fig. 4.2.

The STM system is in an ultra high vacuum (UHV) environment since the spectroscopic measurement is sensitive to contamination by air. Fig. 4.3 shows pictures of the chambers used in this study. The UHV STM system has a main chamber, a sample insertion chamber, and a magnetic linear motion manipulator, as shown in Fig. 4.4. The main chamber is a stainless steel six way cross with 8” conflat flanges, pumped by a 120 liter/sec ion pump. The pressure in the main

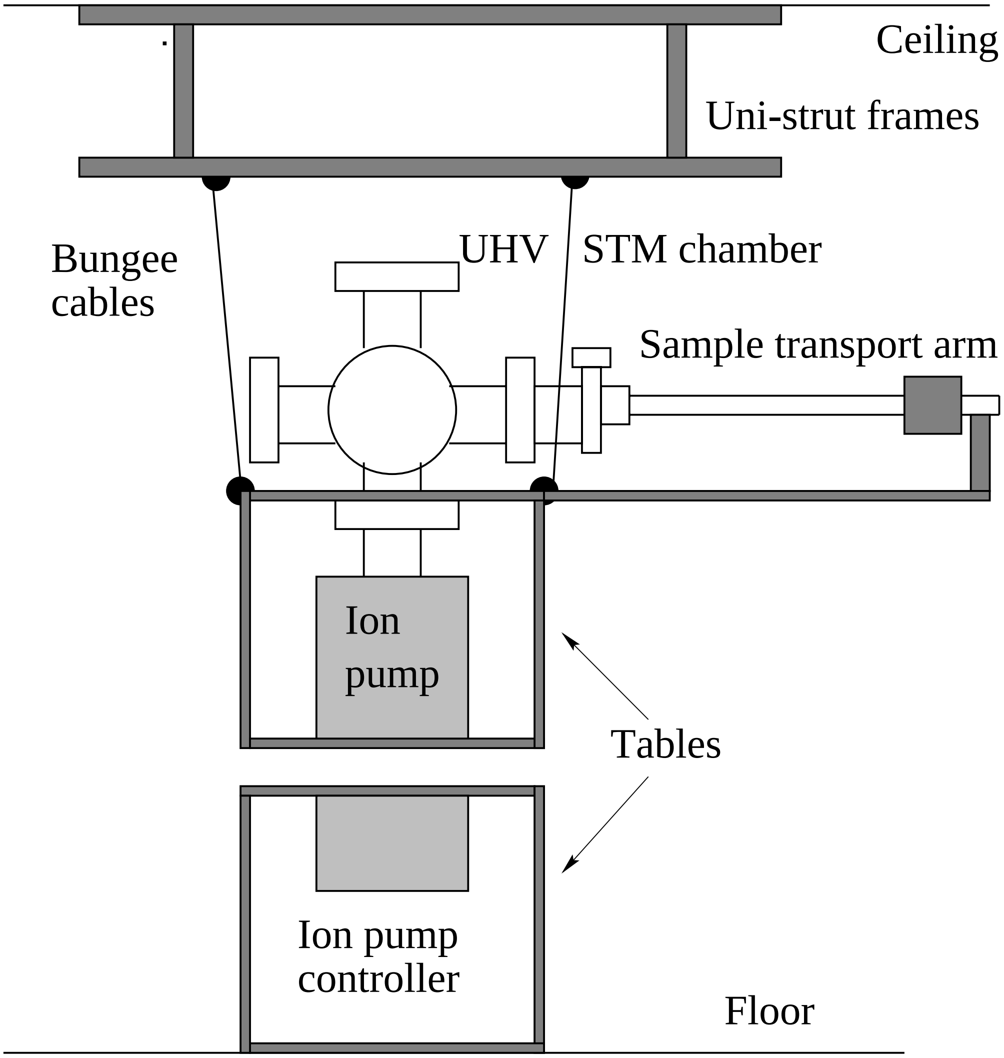


Figure 4.1

A schematic of vibrationless mounting of ultra high vacuum (UHV) STM. The UHV STM chamber is mounted on the upper table. The chamber is hung with the bungee cables during the experiment to isolate the mechanical vibration from the floor and the ceiling.

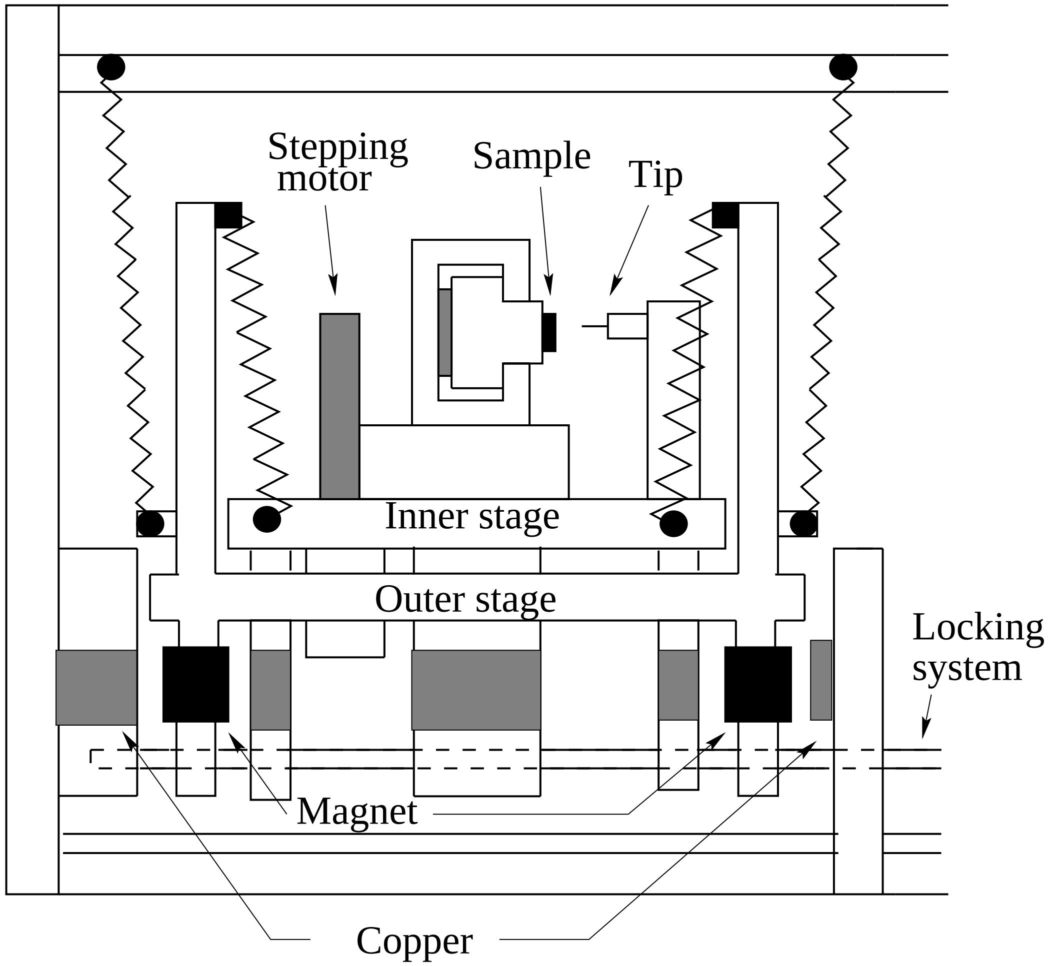


Figure 4.2

A schematic of STM head. The double stage spring suspension system with magnetic eddy-current damping system is used to isolate vibration. Any relative movement between the inner and outer stages of STM head generates an eddy current, which provides a damping force.

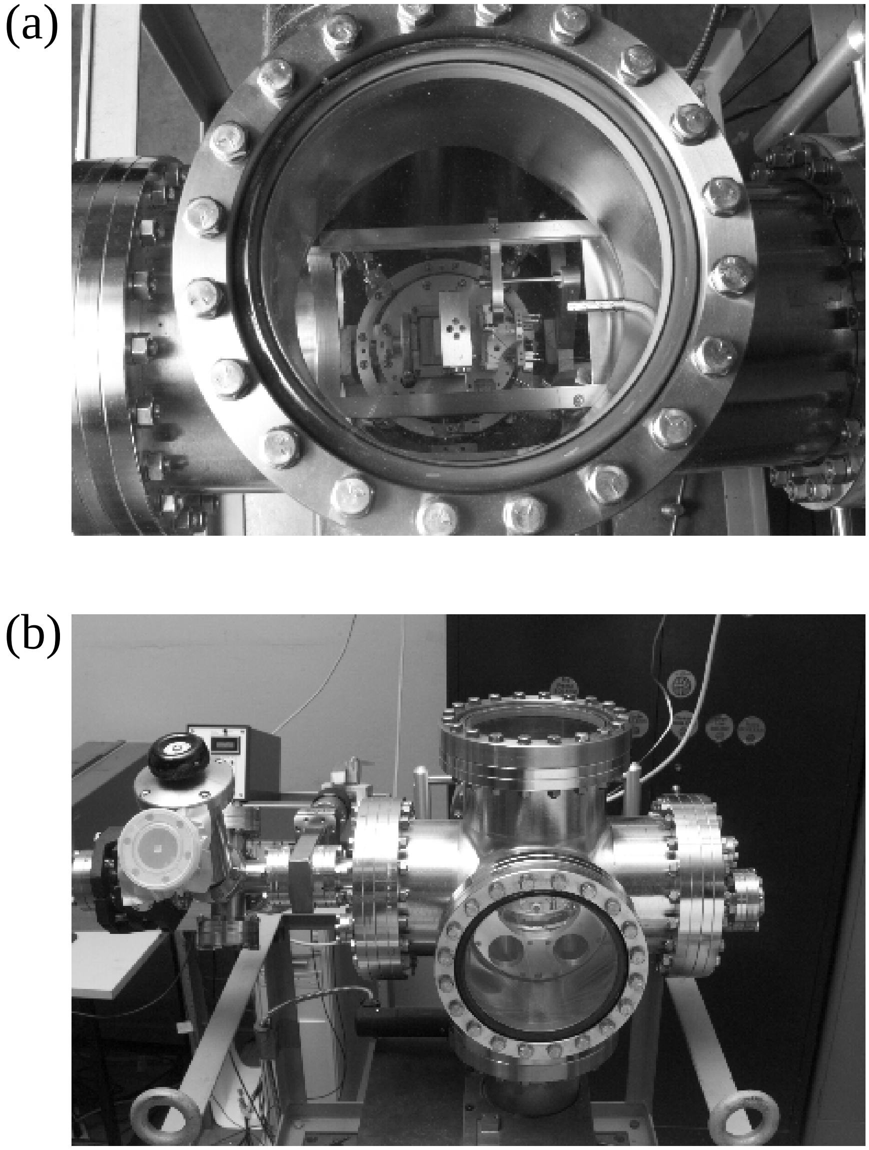


Figure 4.3

Pictures of UHV STM chamber: (a) Top view of main chamber. (b) Side view of main chamber.

chamber is less than 1×10^{-9} Torr as measured by a nude ion-gauge. After a cycle of baking, the pressure can be reduced to 8×10^{-10} Torr. The sample insertion chamber is 2 $\frac{3}{4}$" six way cross which is connected with the main chamber by a gate valve and also connected with the magnetic linear motion manipulator. This chamber can be connected with a turbomolecular pump by another gate valve. A window port of the sample insertion chamber is opened to air in order to insert a sample or tips. After it is pumped using a 110 liter/sec turbomolecular pump, a sample or tips can be inserted into the main chamber using the magnetic linear motion manipulator.

4.2 UHV STM Head

The UHV STM head (Fig. 4.2) is a commercial model of Park Scientific Instruments (Model name: STM-SU2) and modified with a custom designed sample holder and tip transfer kit (see Appendix A, B, and C). The STM head can store six tips and allow *in-situ* tip replacement. New tips can be inserted from outside the chamber without breaking the vacuum.

The STM head has an inner stage and outer stage. A stepping motor, sample holder, and tip holder are on the inner stage. To be as free of mechanical vibration as possible, a magnetic eddy current damping system is used. Any relative movement between the inner and outer stages of STM head generates an eddy current, which provides a damping force.

Tip sample approach is achieved manually and by computer with a vacuum stepping motor attached to the sample positioner.[47] The stepping motor is controlled by a controller (Princeton Research Instrument, Model name: SK-1). One step of the stepping motor is around 150 nm. Since 150 Volt can be applied to the z piezoelectric scanner during the tip sample approach, the available maximum range of the z piezoelectric scanner is 240 nm. (The sensitivity of z piezoelectric scanner is 1.6 nm/V.) There are at least more than one step within the 240 nm in the tip sample approach, hence it is possible to obtain the computerized tip sample approach within the range of a set current. For a STM image, ± 150 Volt can be applied to the x and y piezoelectric scanners, so the maximum size of the STM image is about $0.4\ \mu\text{m} \times 0.4\ \mu\text{m}$. (The sensitivities of x and y piezoelectric scanners are 1.4 nm/V.)

The x and y piezoelectric scanners were routinely calibrated from STM images using the atomic periodicity of highly oriented pyrolitic graphite (HOPG), as shown in Fig. 4.5. In this image, white objects are carbon atoms and spacing between adjacent carbon atoms is 0.25 nm. Only every other carbon atom appears from the real honeycomb structure of HOPG due to a particular symmetry of the wave functions at the Fermi surface near the $\bar{K}$ points in the surface Brillouin zone.[48] The resulting image is a hexagonal closed-packed pattern. Fig. 4.6 shows a smaller size ($2\text{ nm} \times 2\text{ nm}$) and a larger size ($8\text{ nm} \times 8\text{ nm}$) STM image of HOPG in the atomic resolution. Au cluster with a known dimension (4 nm for height) was used for calibration of the z piezoelectric scanner.

4.3 Tip Preparation

The resolution of STM images is closely related to the tip end form. There are several ways to produce sharp tips. One easy way is cutting a Pt-Ir (platinum-iridium) wire with a cutter. The Pt-Ir tips do not oxide as quickly as W (tungsten) tips and can be kept in a storage place within UHV chamber. (The UHV STM chamber can store total six tips and allow *in-situ* tip replacement.) The cut tips may not be well defined in shape and cause a multiple or distorted image. Therefore, it is hard to obtain reliable data in every STM experiment using different tips even on the same sample. The best way to accomplish a reliable result will be changing tips and scanning various spots of the sample surface. Unreliable data due to the tip effect can be easily determined from the STM topographic images with various tips. The Pt-Ir wire used in this study is 0.008” (0.2 mm) in diameter.

Fig. 4.7 shows transmission electron microscope (TEM) micrographs of a STM tip made by cutting a Pt-Ir wire before it is used in STM experiments. (TEM micrographs were taken with Elton Graugnard in Department of Physics, Purdue University.) This tip is not well-shaped and has multiple micro-tips [Fig. 4.7 (a)]. Since the right micro-tip protrudes more than the left micro-tip, the right micro-tip will play the role as the STM tip in experiment unless it is tilted at a significant angle over sample. Zoomed-in pictures taken from the right micro-tip [Fig. 4.7 (b) and (c)] indicate that the end of cut tip can be made sharp with a diameter less than 15 nm.

A second cut tip was studied by TEM after it was used in an STM experiment, as shown in Fig. 4.8. From the zoomed-in picture, this tip appears to be bent after an STM experiment.

Another way to make sharp tips is an electrochemical etching method.[49] Fig. 4.9 shows an optical microscopic photograph and TEM micrographs of tips obtained by this etching method. These etched tips are better shaped in overall than cut tips, but are not so sharp as cut tips. Therefore, producing STM tips by the cutting method is as efficient as etching method. Furthermore, the residuals of chemicals in the etching solutions can reside on the tips and affect the spectroscopic measurement that depends on the both density of states of the tip and sample. Therefore, etched tips were not used often in this study because of these reasons.

4.4 STM Electronics

The block diagram of a feedback circuit for imaging in the constant current mode is presented in Fig. 4.10. The tunneling current signal is converted to the voltage signal by a preamplifier (Keithley 428 current amplifier). Since the high source resistance makes the circuit susceptible to electrostatic coupling (capacitive coupling), the current wire should be kept short. For this reason, the preamplifier should be mounted as close to the tunneling junction as possible in order to minimize the capacitance. The signal output from the preamplifier is linearized by a logarithmic amplifier to improve the dynamic range since the tunneling current is exponentially dependent on the tip sample separation.

The measured tunneling current is compared with the reference current (set current) and the resulting error signal is fed into the main feedback amplifier. The feedback signal is then amplified by a high voltage amplifier and applied to the z piezoelectric scanner to adjust the tip sample separation. For x and y piezoelectric scanner, separate high voltage amplifiers are used to control the scan area.

To perform I-V measurement and other spectroscopic measurements in an analog circuit, a sample-and-hold amplifier is inserted in the circuit just ahead of the main feedback amplifier in order to maintain a fixed tip position. In the hold period, the error signal is set to zero so that the z piezoelectric voltage does not change, maintaining a fixed tip sample separation.

Compared with analog feedback system, digital feedback system contains all the feedback elements in computer programs and allows the computer to control the tip motion directly. The STM system used in this study was retrofitted with controlling electronics and software obtained from Nanotec^{TM}.[50] The Nanotec software was chosen because it employs a fast digital signal processor (DSP) which allows better real-time control of any STM experiment.

Fig. 4.11 is the block diagram of the computerized STM system for STM control, data acquisition, real time display, and image process. The tunneling current is converted by a preamplifier (Keithley 428 current amplifier) with a variable gain typically from 10^6 V/A (1 mV/nA) to 10^8 V/A (100 mV/nA). The converted voltage signal is read by the DSP. The DSP board has 16 bit 4 ADC (analog-to-digital converter) channels and 4 DAC (digital-to-analog converter) channels. The operating voltage of the DSP is ±3 Volt. The DSP runs the feedback loop and takes data independently and the computer displays the data transferred from the DSP on the monitor, allowing a flexible and fast feedback system to be achieved.

The output signal from the DAC of the DSP board is amplified by high voltage amplifiers which amplify the DSP output signal of ±3 Volt up to the range of ±150 Volt. The high voltage amplifiers give seven output signals to the $\pm x$, $\pm y$, and $\pm z$ piezoelectric scanners and bias voltage V_t. The maximum bias voltage is limited to ±12 Volt.

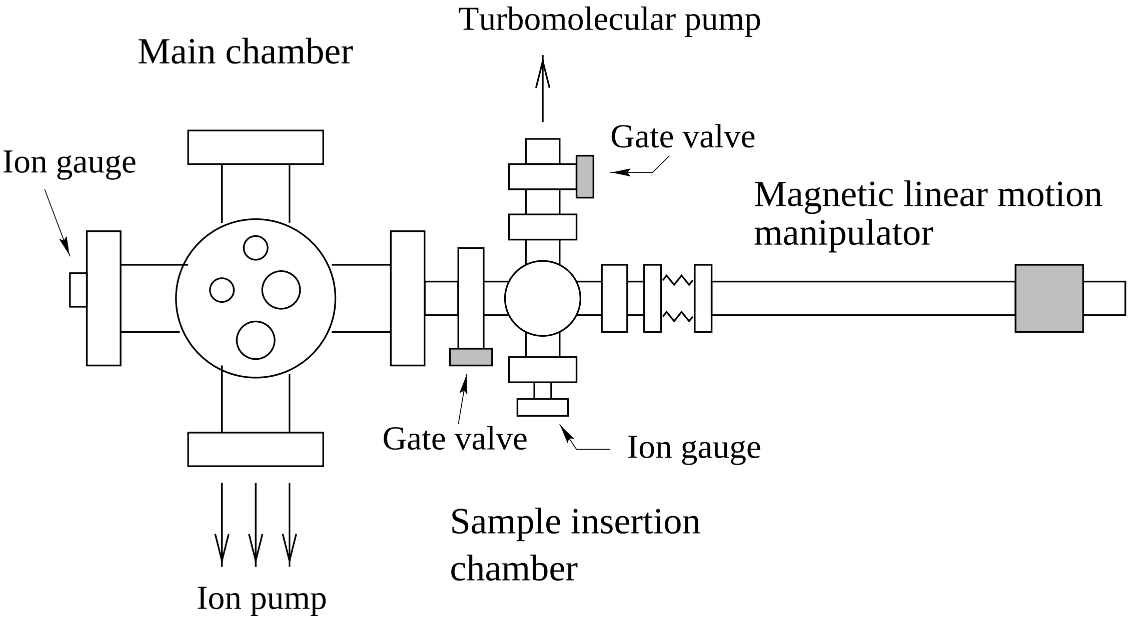


Figure 4.4

A schematic of UHV STM chambers.

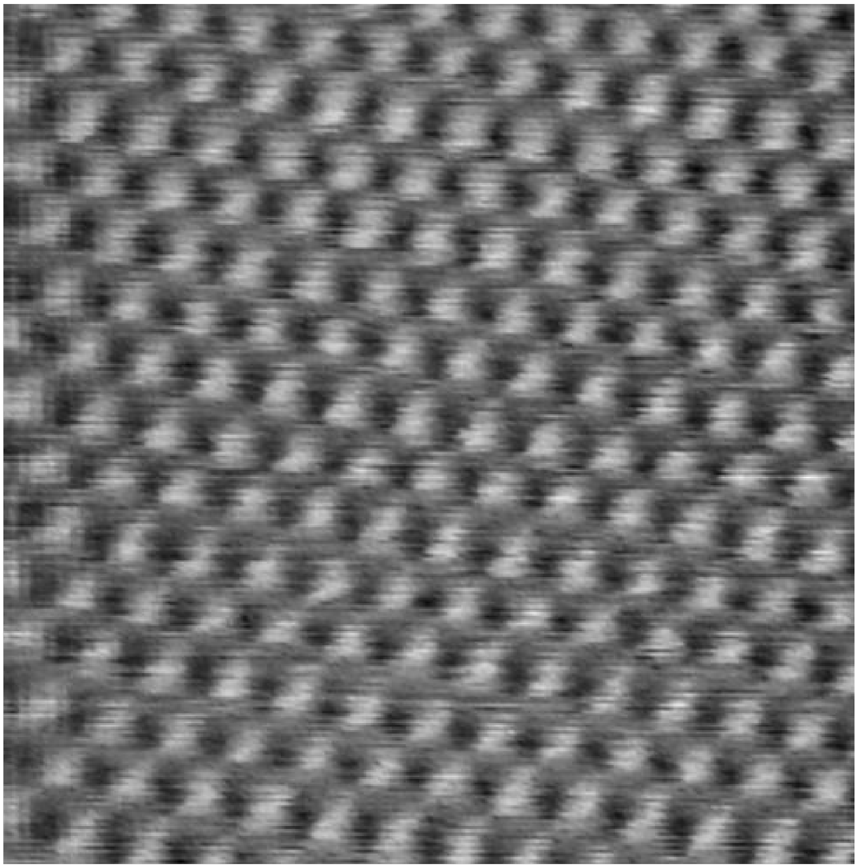


Figure 4.5

A 4 nm × 4 nm STM image in the atomic resolution of highly oriented pyrolitic graphite (HOPG), acquired with a I_{set} of 1.2 nA, a V_{set} of -100 mV, and a scan rate of 41 Hz in the constant height mode.

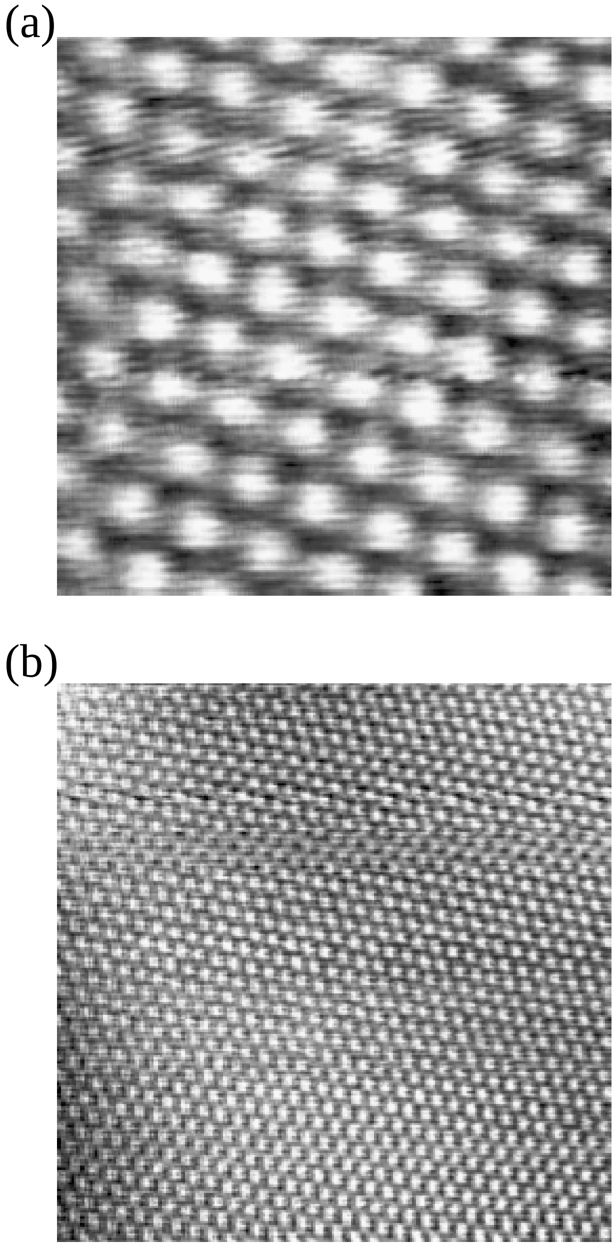


Figure 4.6

(a) A 2 nm × 2 nm STM image of HOPG, acquired with I_{set} = 2.0 nA and V_{set} = -170 mV. (b) A 8 nm × 8 nm STM image of HOPG, acquired with I_{set} = 2.0 nA and V_{set} = -80 mV.

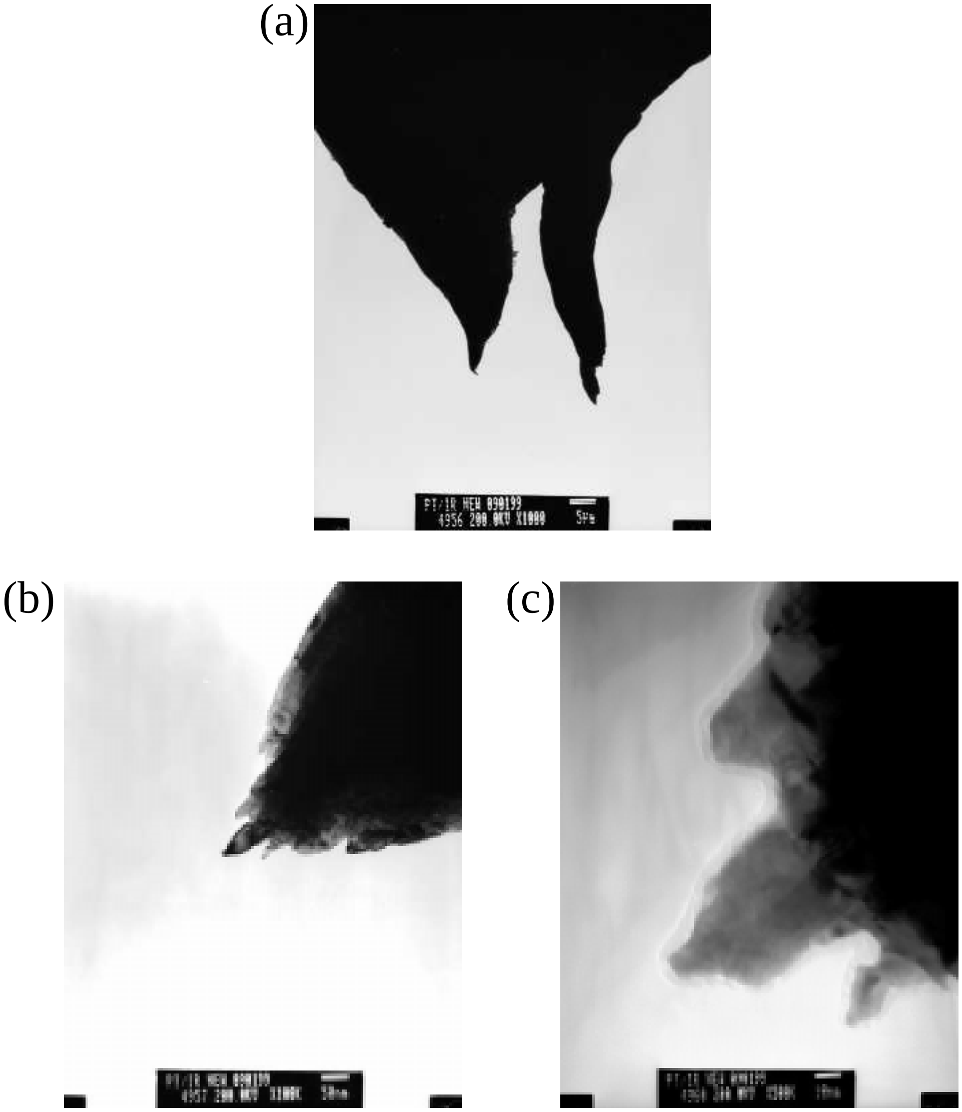


Figure 4.7

Transmission electron microscope (TEM) micrographs of a STM tip made by cutting a 0.008" diameter Pt-Ir wire before it is used in STM experiments: (a) The cut tip is not well-shaped and sometimes it produces multiple micro-tips (scale bar = 5 μm). (b) This image was taken from the right micro-tip seen in (a) (scale bar = 50 nm). (c) Zoomed-in picture of the micro-tip in (b) (scale bar = 10 nm). The end of cut tip can be sharp with a diameter less than 15 nm. Notice that Pt-Ir tip appears to be coated by a thin layer (2-5 nm thick).

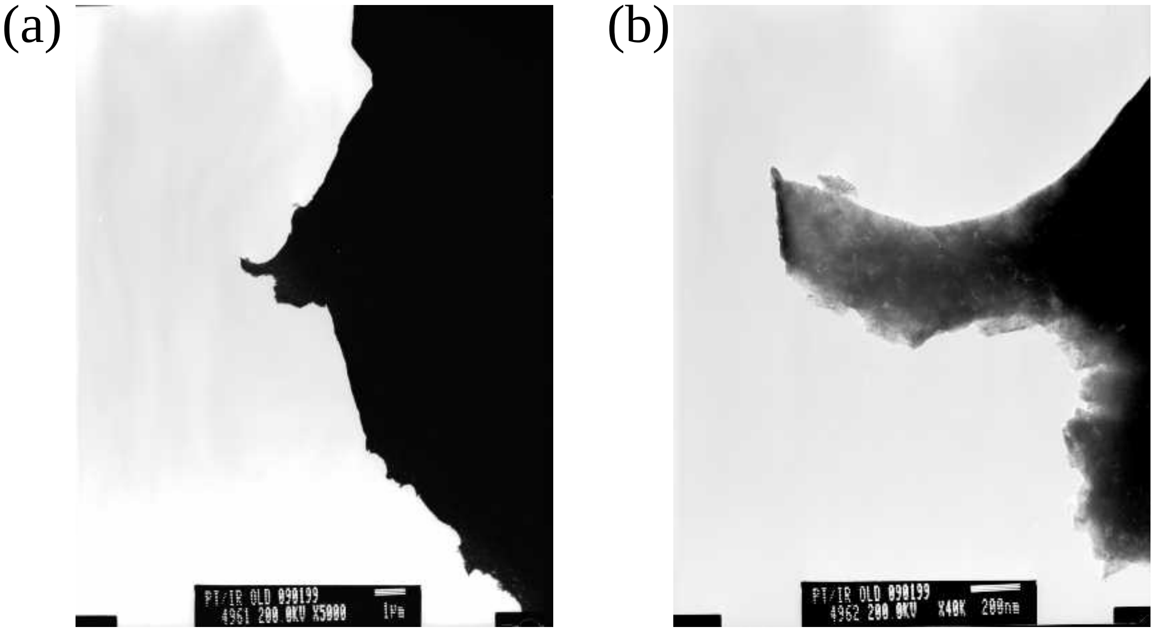


Figure 4.8

TEM micrographs of a STM tip made by cutting a 0.008" diameter Pt-Ir wire after it was used in a STM experiment: (a) It has only one micro-tip at the end (scale bar = 1 μm). (b) Zoomed-in picture of this tip (scale bar = 200 nm). This tip appears to be bent after a STM experiment.

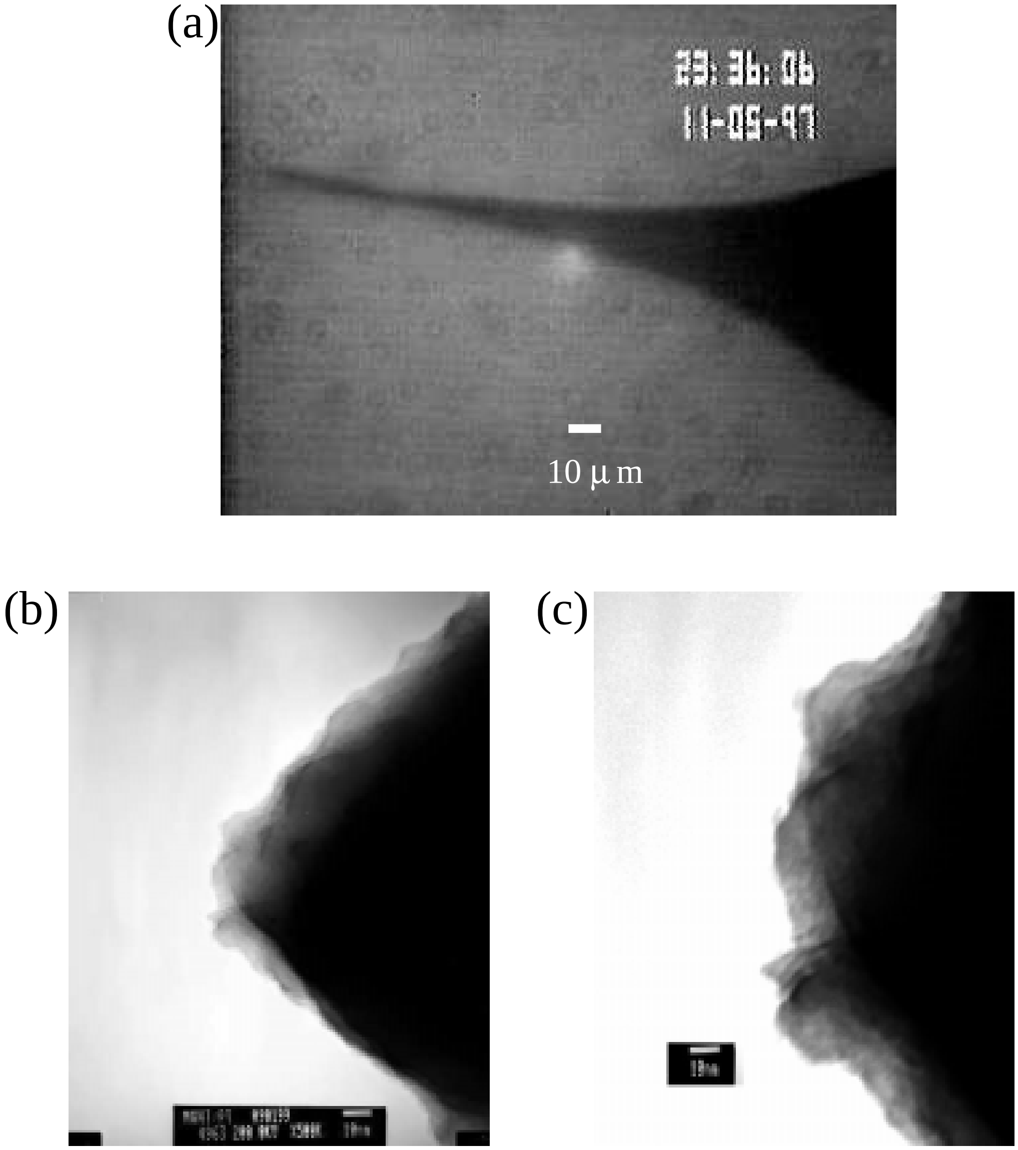


Figure 4.9

(a) An optical microscopic photograph of an etched Pt-Ir tip from a 0.008” diameter Pt-Ir wire. (b) A TEM micrograph of an etched Pt tip from a 0.003” diameter Pt wire (scale bar = 10 nm). (c) Zoomed-in picture of (b) (scale bar = 10 nm).

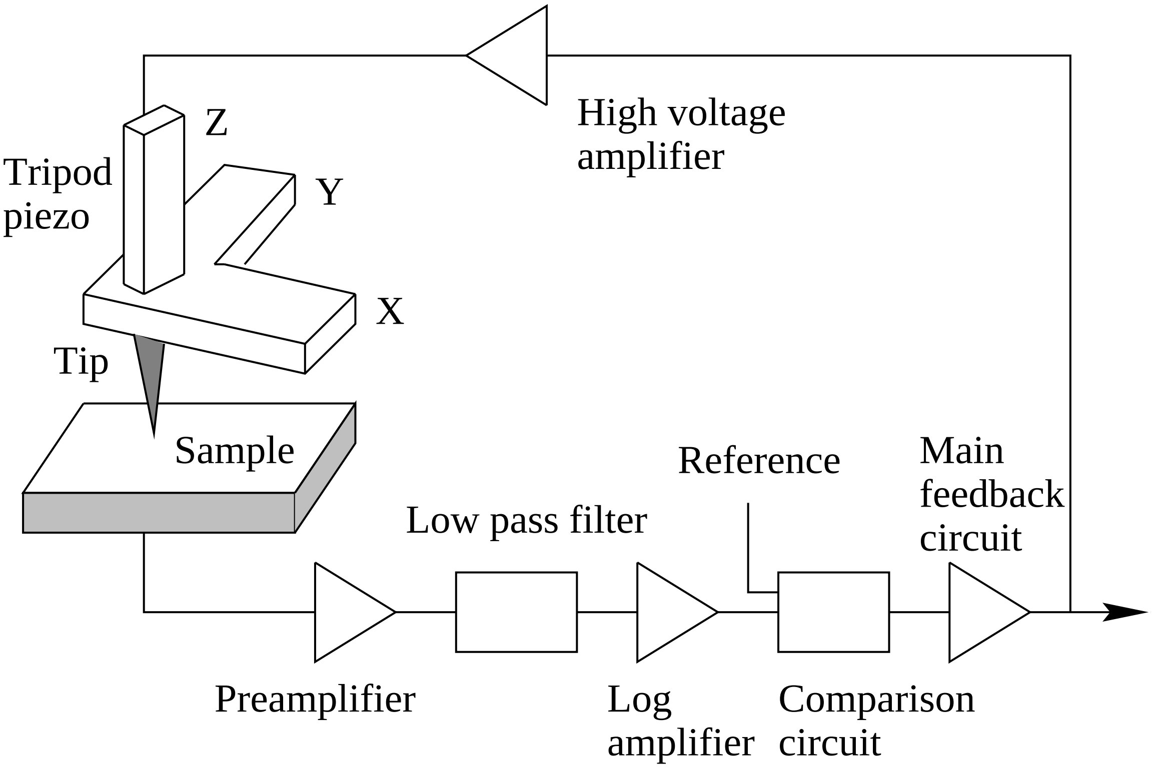


Figure 4.10

Block diagram of feedback loop.

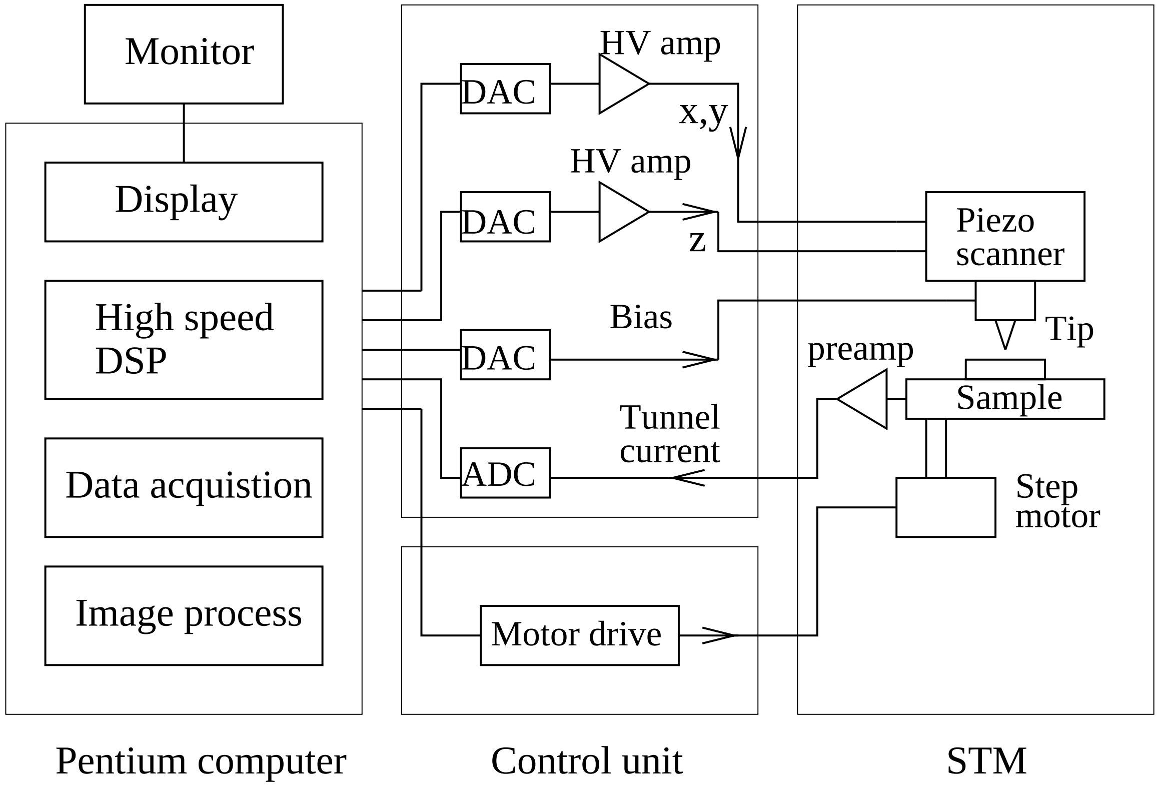


Figure 4.11

Block diagram of the computerized STM system.

5. SELF-ASSEMBLED MONOLAYERS ON GaAs

5.1 Self-Assembled Monolayers

Self-assembled monolayers (SAMs)[29] are molecular assemblies that are formed spontaneously in an ordered way on a substrate by simply immersing the substrate into a solution containing organic molecular compounds. It is widely recognized that SAM can provide a control of individual molecules into ordered structures at the molecular level and therefore can be a potential for nanoscale material applications.

A SAM can be viewed as three parts as shown in Fig. 5.1: (i) head group which provides chemisorption of a molecule onto a substrate resulting in a strong molecule-to-substrate interaction, (ii) bulk group of a molecule, and (iii) terminal group of a molecule. An example of SAM is alkanethiol on gold. (A dodecanethiol [$CH_3(CH_2)_{11}SH$] is shown in Fig. 5.1: Dodecanethiol is one of alkanethiol molecules.) In this case, head group is thiol (sulfur) which provides a strong S-Au bonding, bulk group is alkyl chain [$(CH_2)_n$] of hydrocarbon molecules, and terminal group is methyl (CH_3) group. Due to the strong head group-to-substrate interaction, molecules can occupy every available binding site on the substrate and form an ordered close-packed structure. A hexagonal close-packed structure

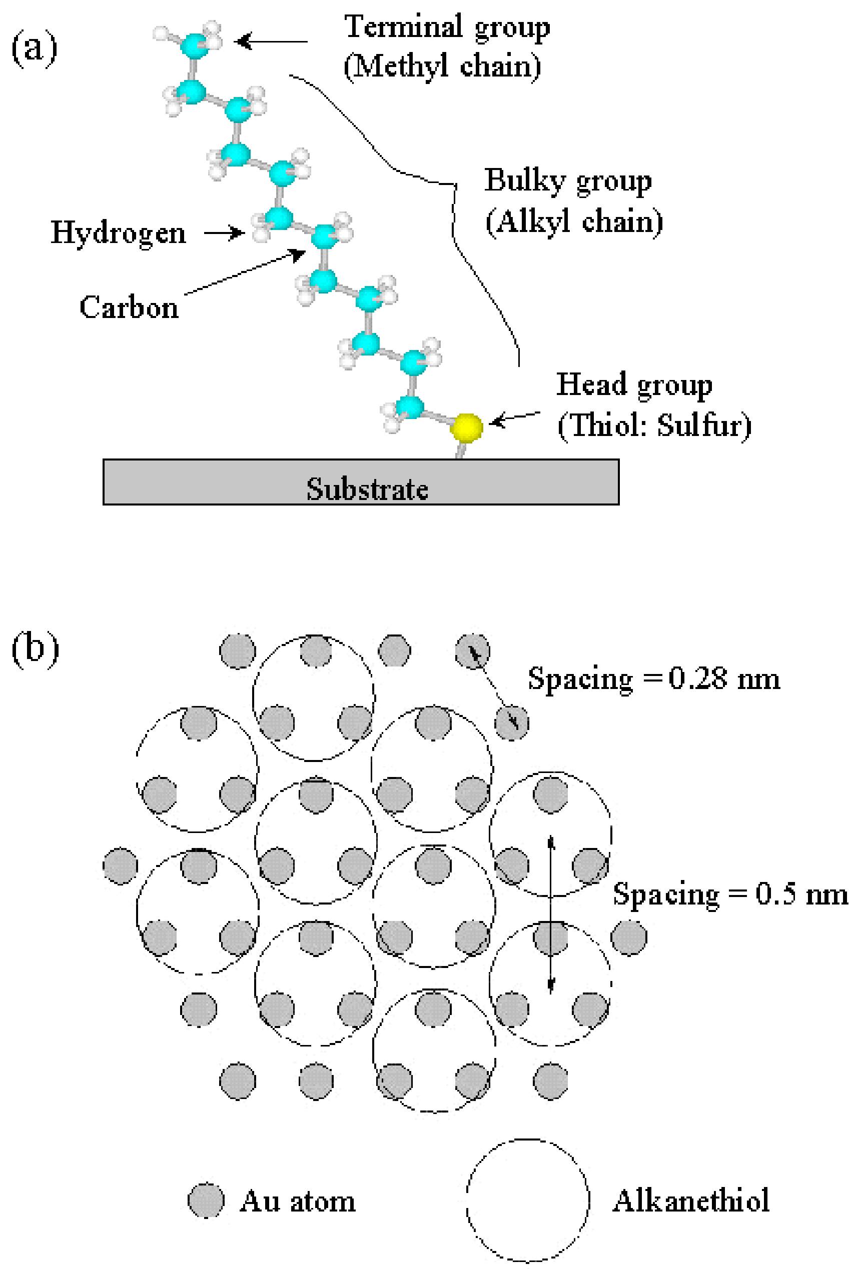


Figure 5.1

(a) A schematic view of a SAM consisting of head group, bulk group, and terminal group. The molecule is dodecanethiol with head group of thiol, bulk group of alkyl chain, and terminal group of methyl group. (b) A schematic illustrating hexagonal close-packed structure of an alkanethiol SAM on Au(111).

of alkanethiol SAM on Au(111) has been observed using STM and AFM in the molecular resolution.[51–53]

SAM is of great interest due to the variety of chemical synthesis. For example, different head group can be used to bond onto different substrate, such as alkanethiols on Au[51–53] and alkyltrichlorosilanes on SiO_2/Si.[54] Phenyl group can be used as bulk group of SAM instead of alkyl chain to increase current conduction. Furthermore, by introducing a certain terminal group, it will play a role as a tether molecule. A molecule with both thiol end groups as head and terminal group can tether Au cluster onto Au substrate.[5] Therefore, SAM has a potential for materials and electronics application at the molecular scale.

In most cases SAM has been successfully formed on metallic substrates or oxidized substrates. However, semiconducting substrates have a relevance of future electronic devices because semiconductor device layers can provide device functionality such as the gain essential for regenerative logic functions and directionality. Therefore, the integration of SAM on semiconductor substrate is of particular interest. This chapter will discuss the formation of SAM on a semiconductor (GaAs).

5.2 Low Temperature Grown GaAs

GaAs is one of the major compound semiconductor materials. GaAs has made a significant impact on the world of Si-based electronics due to the special features of GaAs, for example, the ability to form lattice perfect heterojunction structures with AlGaAs and high electron mobility in GaAs. However, GaAs can't be used in air because the presence of oxygen on the GaAs surface leads to the formation of both gallium oxide (Ga_2O_3) and arsenic oxide (As_2O_3) quickly (in seconds).[55,56] The oxidation process is accelerated in the presence of light because light generates electron-hole pairs and holes accelerate oxidation process.[57] The chemical passivation of GaAs surface to prevent oxidation has been studied involving elemental sulfur[58–60] and thiol molecules.[61–63] It has been reported that the chemical passivation with thiol molecules modified the barrier height of GaAs Schottky diode, reduced non-radiative surface recombination rate, and improved the photoluminescence (PL) signal. It is believed that the thiol to GaAs bond provides passivation comparable to that observed in studies involving elemental sulfur.

Recently, GaAs grown by MBE at a low temperature of 250-300 °C (LTG:GaAs) has been known to be more resistive to oxidation than GaAs grown at a normal temperature of 600 °C.[64] X-ray photoemission spectroscopy (XPS) measurements of undoped LTG:GaAs indicate that the time constant for significant oxidation of the surface is longer than one hour at atmosphere.[64] (GaAs generally oxidizes in seconds.) This property is due to a relative low concentration of minor carriers (holes) in the surface layer arising from the small minority carrier lifetime in LTG:GaAs material.[64,65] LTG:GaAs has been of great interest since LTG:GaAs shows a lot of interesting electrical properties associated with roughly 1-2 % excess arsenic concentration incorporated during growth, resulting in a high concentration ($\sim 1.0 \times 10^{20}$ cm^{-3}) of point defects due to arsenic antisite defects.[27,28] Fig. 5.2 is a model structure of LTG:GaAs where it contains an arsenic antisite defect (As_{Ga}).

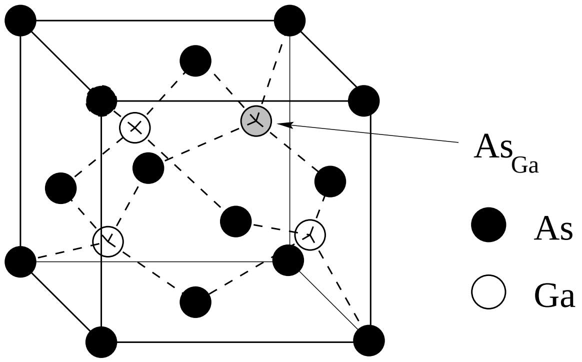


Figure 5.2

Model structure of LTG:GaAs. It contains an arsenic antisite defect (As_{Ga}).

For as-grown LTG:GaAs material, the Fermi level is pinned near midgap, which is attributed to the arsenic-related point defects (see Fig. 7.1).[27] Feenstra, et al. used STM to image arsenic-related defects in *in-situ* cleaved LTG:GaAs(110) and these defects resulted in a band of midgap states within the energy bandgap.[66] For an undoped LTG:GaAs layer (n-type), this band of midgap states was located about 0.5 eV above the valence band edge of the material. This band has been observed in a LTG:GaAs(100) sample which was exposed to air for 20 minutes and also observed after the sample was stored in a nitrogen filled desiccator for 1 day.[65] When LTG:GaAs is annealed at 600-800 °C, arsenic precipitates are observed with diameters of 5-15 nm.[67]

Another interesting property of LTG:GaAs is that this material can be used for high performance ohmic contact. Patkar, et al. have reported that the specific contact resistance to n-GaAs(100) having LTG:GaAs surface layer can be below

1×10^{-6} $\Omega\cdot$cm^2.[68] This ohmic contact behavior is associated with arsenic antisite defect assisted tunneling through thin LTG:GaAs layer and tunneling through a thin barrier due to the space charge region of heavily doped GaAs layer (Si at 1×10^{20} cm^{-3}). Unlike conventional alloyed contacts such as Au/Ge/Ni on n-type GaAs, this nonalloyed contact employing LTG:GaAs is appropriate for the nanometer scale device applications since it will not suffer from a deep interface and spatial nonuniform alloying found in Au/Ge/Ni alloyed contacts.[69]

The GaAs layer structure used in this study, shown in Fig. 5.3, employs a thin (10 nm) layer of LTG:GaAs to facilitate a high quality ohmic nanocontact to n-GaAs(100) layers grown at standard temperatures. Two wafers were prepared with the same vertical structures except for the doping in the LTG:GaAs cap layer: one is undoped LTG:GaAs (n-type) and the other is Be-doped LTG:GaAs (Be-doped at 2×10^{20} cm^{-3}). Be-doped LTG:GaAs is still n-type (upward band bending) as a consequence of the large number of donor-like defects (arsenic antisite defects). The doped layers (n++ and n+ Si-doped GaAs layers) were grown at the typical GaAs growth temperature of 580 °C. The LTG:GaAs layer was grown at 250 °C in order to incorporate excess arsenic. The growth rate was 1 μm/hour. [Samples were grown by M.R. Melloch and E.H. Chen (currently at Yale University) in School of Electrical and Computer Engineering, Purdue University.]

The second layer (n++ GaAs layer) is important in the low resistance ohmic contact structure. Highly activated donor density (1×10^{20} cm^{-3}) in this layer results in a thin barrier for electron conduction when a metal contact is made.

10 nm	LTG:GaAs (undoped/Be-doped)
10 nm	n++ Si doped GaAs (10^{20} cm^{-3})
50 nm	n+ Si doped GaAs (5 x 10^{18}cm^{-3})
	n+ GaAs(100) substrate

Figure 5.3

A schematic of the GaAs layer structure for ohmic contact.

The activated donor density is dependent on the amount of Si incorporated during the growth, but the dependence is not linear because of the limit on a ratio (solid-solubility) of activated donor density to the amount of Si incorporated during the growth for the stoichiometric GaAs. This doping limit (bulk amphoteric doping limit) in stoichiometric GaAs is $\sim 5 \times 10^{18}$ cm^{-3}. This problem can be overcome using a thin LTG:GaAs cap layer on top of GaAs due to the Fermi level control, and much higher activated donor density (1×10^{20} cm^{-3}) can be obtained.[68]

Before any molecules are applied to the surface of LTG:GaAs, an as-grown undoped LTG:GaAs was examined first by a root mean square (rms) surface roughness determined from the UHV STM topographic image spanning 100 nm × 100 nm. (Samples were typically exposed to air for 15-20 minutes during the transfer to UHV STM appratus from MBE growth chamber.) The rms value for as-grown undoped LTG:GaAs was found to be around 0.4 nm (see Table 5.1). Fig. 5.4

shows the schematic of STM operation and a topographic image of an undoped LTG:GaAs sample. STM spectroscopic measurements can be performed on the LTG:GaAs sample simultaneously with topographic imaging (known as CITS technique). Fig. 5.5 shows the results of I-Vs on two different regions of the topographic image of undoped LTG:GaAs [Fig. 5.4 (b)]. The I-V characteristic in the region A of the topographic image revealed an enhanced conduction behavior [Fig. 5.5 (a)]. Contrary to the region A, the I-V characteristic in the region B showed a wide bandgap [Fig. 5.5 (b)]. The different feature of I-Vs in two regions can be explained by an enhanced conduction due to the midgap states; region A has a high density of midgap states and region B has a less density of midgap states. The region A was a little rougher than the region B, which was probably caused by the incorporation of excess arsenic during the growth at a low temperature.

The energy bandgap in I-V characteristics from two regions can be determined more accurately using $(dI/dV)/(I/V)$ curves. $(dI/dV)/(I/V)$ curves in two regions are plotted in Fig. 5.6. In both cases, the apparent bandgap appears to be less than GaAs energy bandgap. By following a way to determine the energy bandgap from $(dI/dV)/(I/V)$ curves,[65] region A and B have the apparent bandgap of $\sim$ 0.24 eV and $\sim$ 0.93 eV, respectively as compared with the GaAs bandgap of 1.4 eV (also see Table 6.1).

Unlike an early study[65] when about 80 % of scanned area showed signals due to high density of midgap states, only approximately 10-20 % of the scanned area exhibited the enhanced conduction behavior in the current study. This inconsis-

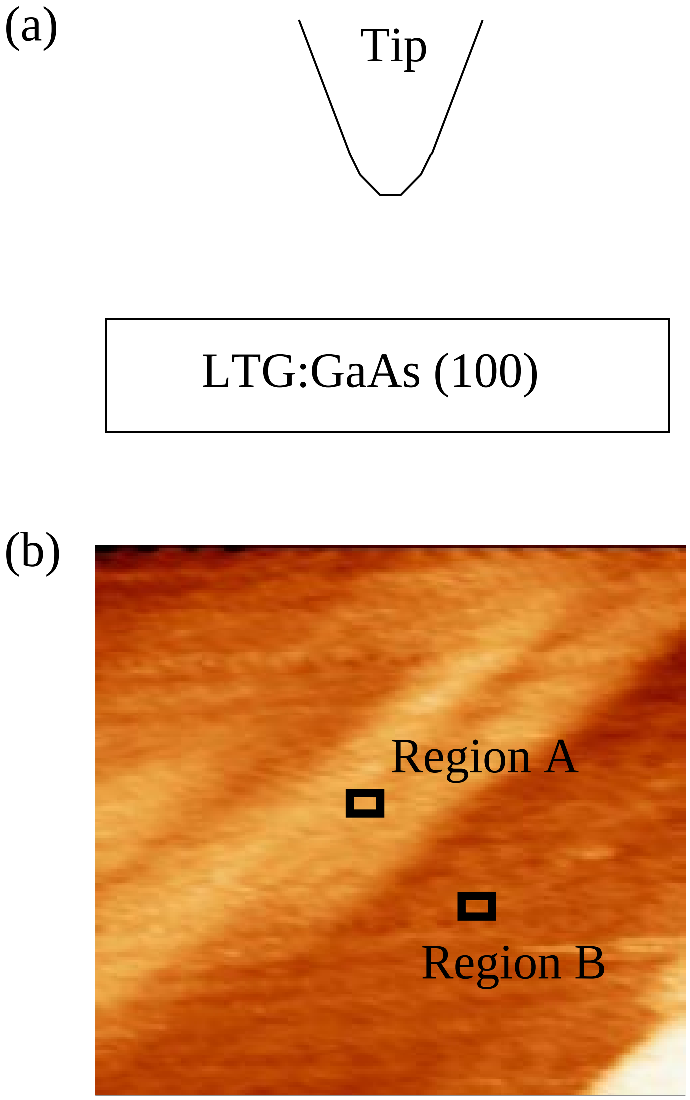


Figure 5.4

(a) A schematic of STM operation on LTG:GaAs. (b) A 30 nm × 30 nm UHV STM topographic image of an undoped LTG:GaAs, acquired with I_{set} = 1.0 nA and V_{set} = -1.0 V.

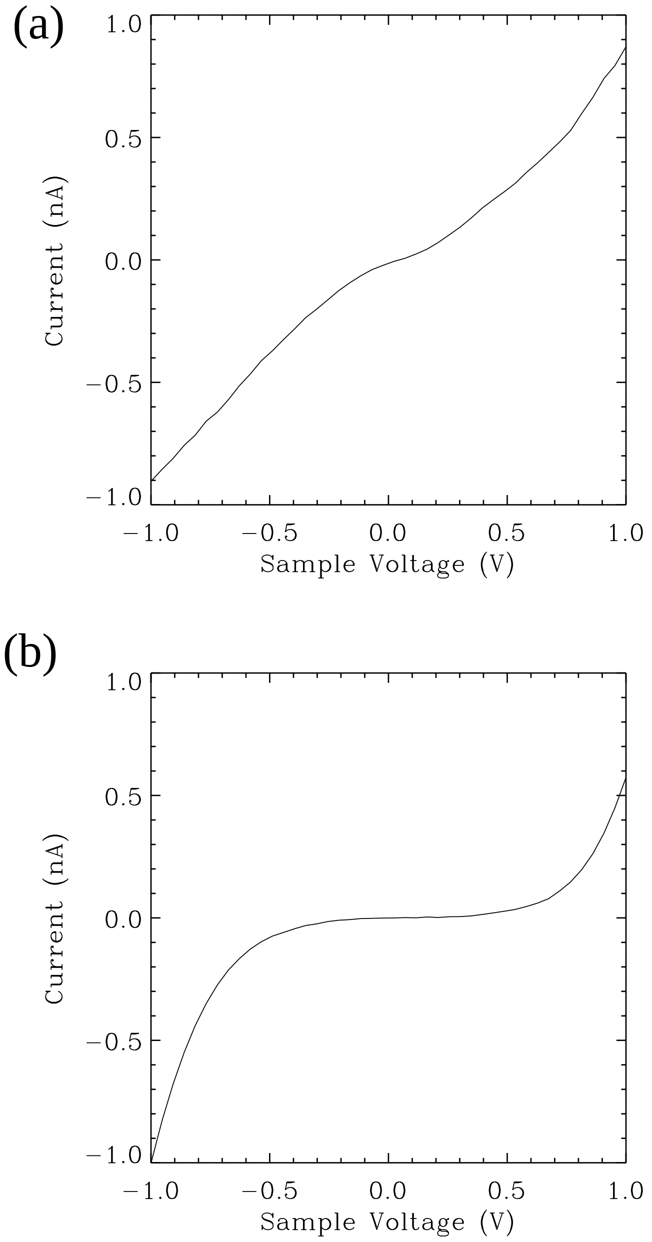


Figure 5.5

I-*V* data on two different regions of undoped LTG:GaAs in Fig. 5.4. (a) *I*-*V* from region A with a high density of midgap states. (b) *I*-*V* from region B with a low density of midgap states. There is a significant enhancement of conduction on the region A due to large amount of midgap states.

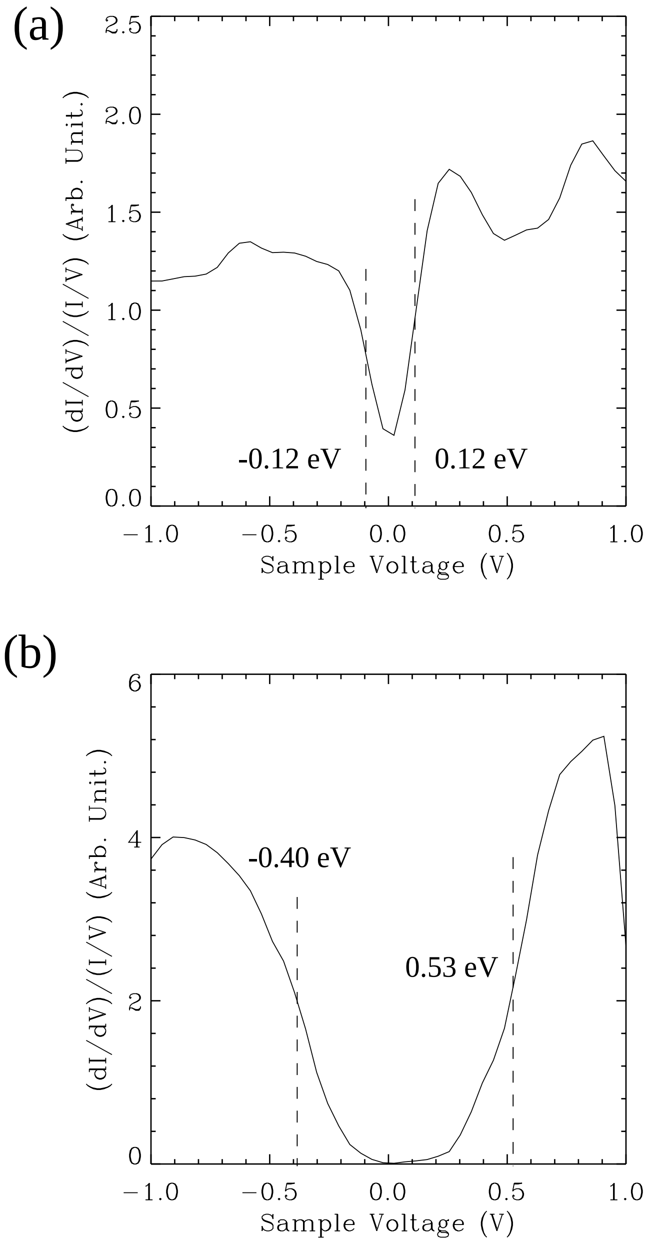


Figure 5.6

$(dI/dV)/(I/V)$ on two different regions of undoped LTG:GaAs in Fig. 5.4. (a) $(dI/dV)/(I/V)$ from region A with an apparent bandgap of $\sim$ 0.24 eV. (b) $(dI/dV)/(I/V)$ from region B with an apparent bandgap of $\sim$ 0.93 eV. Both cases have an energy bandgap less than that of GaAs (1.4 eV).

tency may be attributed to the sensitive dependence of midgap states density on growth temperature of LTG:GaAs and other growth and environment conditions. Also this nonunformity can be a problem for nanometer scale device applications. To overcome this problem, a totally new approach was developed. For this new approach, well-controlled geometry Au clusters having 4 nm diameter were deposited on LTG:GaAs using XYL as a tethering molecule of Au clusters on LTG:GaAs, and these Au cluster were used as an ohmic contact. Before depositing Au clusters, LTG:GaAs samples coated with various molecules were examined, which is discussed in the next section.

5.3 SAM Coated LTG:GaAs

SAMs were grown on LTG:GaAs by two methods. For a SAM of octadecanethiol [$CH_3(CH_2)_{17}SH$, denoted as ODT], LTG:GaAs is immersed in molten thiol ODT for several hours in a dry nitrogen atmosphere and the surplus ODT is washed off using ethanol.[70] [ODT was coated on LTG:GaAs with this method by Venkat Kolagunta (Currently at Motorola) in School of Electrical and Computer Engineering, Purdue University.] For a SAM of dodecanethiol [$CH_3(CH_2)_{11}SH$, denoted as DDT] or xylyl dithiol ($HS\text{-}CH_2\text{-}C_6H_4\text{-}CH_2\text{-}SH$, denoted as XYL), LTG:GaAs is soaked in a 1 mM solution of DDT or XYL in an organic solvent (ethanol or acetonitrile) for 12-18 hours in a dry nitrogen atmosphere. (DDT or XYL was coated on LTG:GaAs by Jia Liu in School of Chemical Engineering, Purdue University.)

The energy difference between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) of a molecule, is known as the HOMO-LUMO bandgap. The XYL molecule has an expected HOMO-LUMO bandgap of 2-6 eV, while DDT or ODT has a large bandgap of 8-12 eV (see Fig. 5.7). Since XYL is electrically more conductive than DDT or ODT, XYL is called a conjugated (conducting) molecule and is a candidate for a molecular wire. On the other hand, DDT and ODT are referred to as a non-conjugated (non-conducting) molecule which serves as a resistive layer. The molecular structures and physical properties of ODT, DDT, and XYL are summarized in Fig. 5.7.

Before applying a SAM on the surface of LTG:GaAs, any residual oxide layer on the surface was first removed by a brief rinse in HCl. A SAM was deposited, the samples were then thoroughly rinsed in solvents and de-ionized water. Several samples were first examined by atomic force microscopy (AFM) (performed by Jia Liu), air STM, and UHV STM. To minimize the oxide contamination, AFM and air STM experiments were done immediately after SAM was grown. For the UHV STM experiment, the sample was inserted into the sample insertion chamber and pumped out with a turbomolecular pump, and then inserted into main chamber having a pressure less than 1×10^{-9} Torr.

Root mean square (rms) value of surface roughness is a good estimator of surface morphology and it is summarized in Table 5.1. Generally, the roughness is less in AFM than in STM since the STM image of a surface contains information of both the surface topography and local electrical conductivity. The presence of

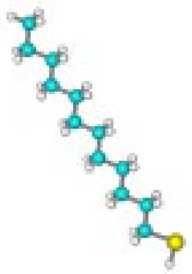
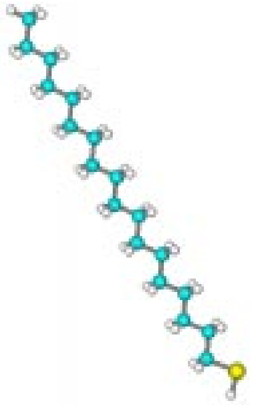
Name	DDT	ODT	XYL
Picture			
Length	1.6 nm	2.3 nm	0.8 nm
Width	0.3 nm	0.3 nm	0.5 nm
HOMO-LUMO Gap	11 eV	11 eV	4 eV

Figure 5.7

Molecular structure and physical properties of DDT, ODT, and XYL obtained using a program (HyperChem).

Table 5.1

RMS roughness of undoped LTG:GaAs surfaces with and without SAM determined from AFM and STM images with sizes of 100 nm × 100 nm. The size of AFM image for XYL/LTG:GaAs is 1 μm × 1 μm.

Sample	Characterization method	RMS roughness (nm)
LTG:GaAs	air AFM	0.21
LTG:GaAs	air STM	0.88
LTG:GaAs	UHV STM	0.42
DDT/LTG:GaAs	UHV STM	1.40
ODT/LTG:GaAs	UHV STM	1.60
XYL/LTG:GaAs	air AFM	1.59
XYL/LTG:GaAs	UHV STM	0.71

nonuniform and poorly conducting oxide regions on a flat surface would appear as variations in a STM image because the STM tip should move towards the surface of oxide regions to maintain a constant tunneling current. It is clear that the roughness in a UHV STM image is less than in an air STM image because there is relatively little contamination in the UHV chamber. The surface of the SAM coated LTG:GaAs is rougher than the original LTG:GaAs. Since the roughness becomes bigger as the scan size of the image increases, the AFM image with a size of 1 μm × 1 μm is rougher than the UHV STM image with a size of 100 nm × 100 nm for XYL/LTG:GaAs. It is interesting, however, XYL-coated LTG:GaAs shows a smaller roughness than DDT or ODT coated LTG:GaAs probably due to the fact that XYL is smaller in length than DDT and ODT (see Fig. 5.7).

Representative samples of the as-grown LTG:GaAs and the XYL-coated LTG: GaAs layers were also characterized using ellipsomicroscopy for surface imaging (EMSI),[71] an ellipsometric imaging technique with submonolayer sensitivity and a spatial resolution of $\sim$ 3 μm (performed by J. Lauterbach's group in School of Chemical Engineering, Purdue University). EMSI can characterize the uniformity and stability of a thin (monolayer) coating as a function of position and time. The EMSI images on as-grown undoped LTG:GaAs indicated that the optical properties (i.e. complex refractive index) varied with time, which can be attributed to a slow and uneven oxidation of the LTG:GaAs surface. The XYL-coated LTG:GaAs surface was observed to be uniform and stable, with no significant change in the EMSI images detected during several hours of exposure to atmosphere. Using reliable values for the optical constants of the substrate and adlayer, EMSI allows a quantitative measure of the thickness of the XYL layer. The EMSI images did reveal a striking spatial uniformity of the ellipsometric signal that suggests the presence of a uniform, monolayer coverage of XYL on the LTG:GaAs.

Fig. 5.8 shows the schematic of STM operation and a topographic image of XYL-coated undoped LTG:GaAs. Like LTG:GaAs material (see Fig. 5.5), two different types of I-V were observed. The I-V curve in the region B of the topographic image has a wider bandgap compared to the I-V curve in region A, as shown in Fig. 5.9. This difference of I-V shape is also attributed to the difference in the amount of the midgap states. Similarly in LTG:GaAs material (see Fig. 5.6), the apparent bandgap of XYL-coated LTG:GaAs appears to be less than GaAs bandgap as shown in Fig. 5.10. Region A and B have the apparent bandgap of $\sim$ 0.53 eV and $\sim$ 1.2 eV, respectively. I-V characteristics measured on LTG:GaAs and XYL/LTG:GaAs are summarized in Table 6.1.

There have been many arguments on where the thiol end group bonds on GaAs. From studies of the elemental sulfur passivation on GaAs, some people reported that sulfur atom bonded only with arsenic site of GaAs,[59] but others observed sulfur bonding both with gallium and arsenic.[72,73] Thiol group (-SH) is negatively polarized and thus may tend to bond with a positively charged ion, in this case gallium site because electron is transferred partially from gallium to arsenic due to the electronegativity difference (1.82 for Ga and 2.20 for As). But there is still no agreement on bonding position of thiol end group. For example, H. Ohno, et al.

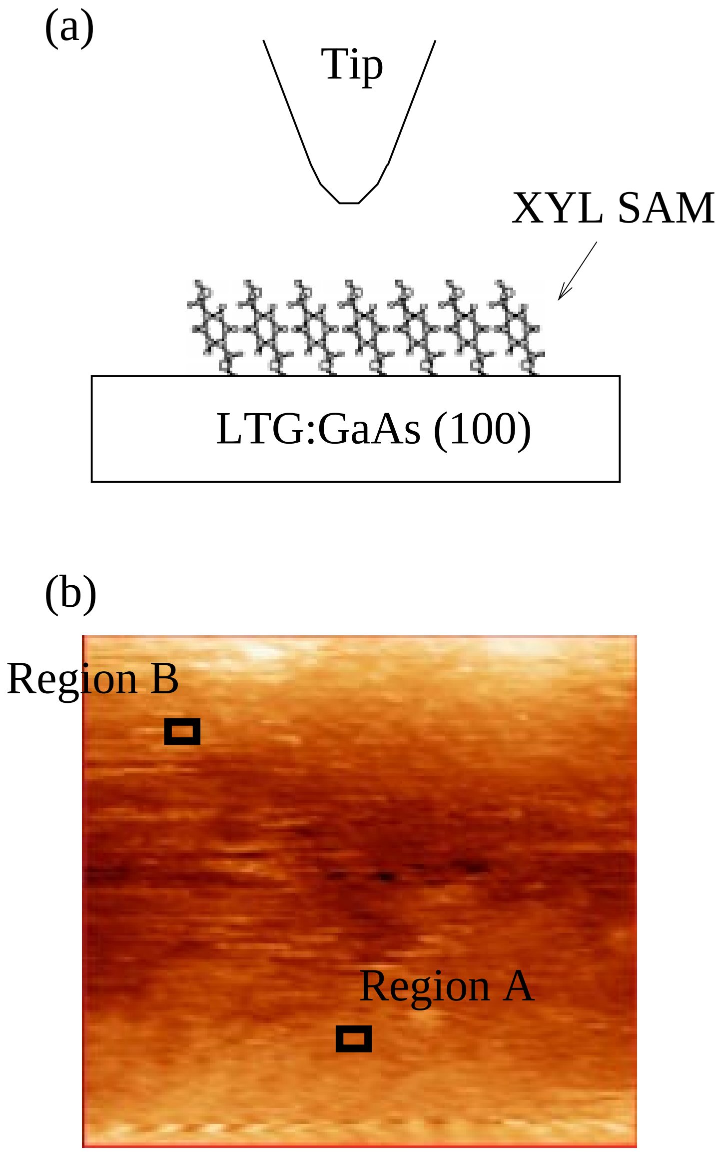


Figure 5.8

(a) A schematic of STM operation on XYL-coated LTG:GaAs. (b) A 40 nm × 40 nm UHV STM topographic image of XYL-coated undoped LTG:GaAs, acquired with I_{set} = 0.8 nA and V_{set} = -1.2 V.

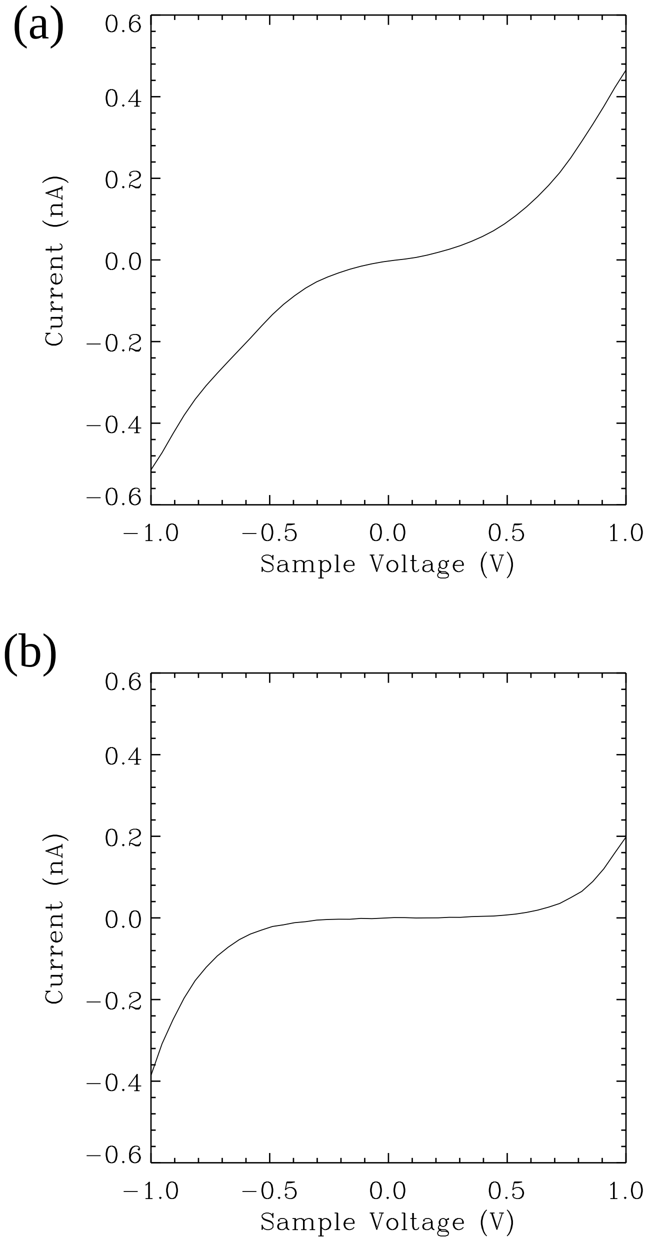


Figure 5.9

I-*V* data on two different regions of XYL-coated undoped LTG:GaAs in Fig. 5.8. (a) *I*-*V* from region A with a high density of midgap states. (b) *I*-*V* from region B with a low density of midgap states. The *I*-*V* shape difference is attributed to the difference in the amount of the midgap states.

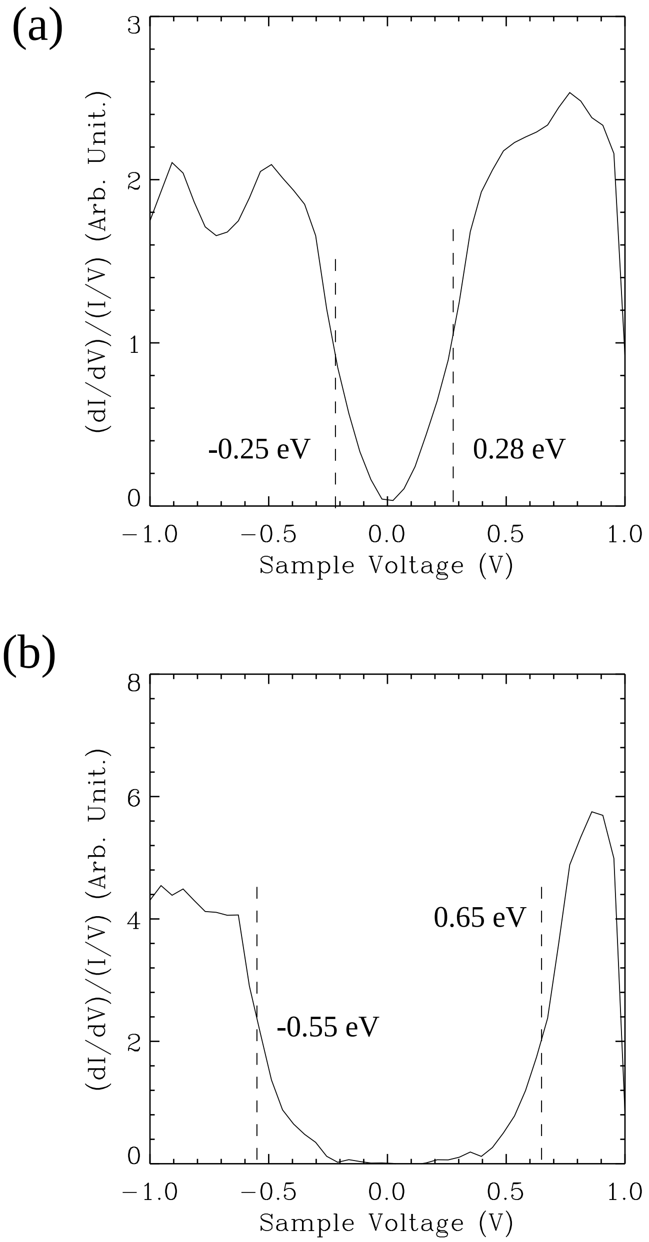


Figure 5.10

$(dI/dV)/(I/V)$ on two different regions of XYL-coated undoped LTG:GaAs in Fig. 5.8. (a) $(dI/dV)/(I/V)$ from region A with an apparent bandgap of ~ 0.53 eV. (b) $(dI/dV)/(I/V)$ from region B with an apparent bandgap of ~ 1.2 eV.

argued that the thiol molecule might bond with arsenic.[74] In the case of Au(111) substrate, the thiol end group is known to sit on the center of three Au atoms.[51]

6. NANOMETER SCALE OHMIC CONTACT ON GaAs

6.1 Introduction

There have recently been numerous examples of prototype electronic devices having nanometer scale dimensions.[75–77] A requirement of many of these nano-devices is the presence of nearby contacts having dimensions of order 1 μm or greater. Thus, even though the device has shrunk well into the nanometer scale, the contacts to the device still require areas $\sim 10^2 - 10^4$ greater than the active device. Nanocontacts having dimensions comparable to a nano-device will be required to alleviate this difficulty in the future.

The demands on nanocontacts are quite stringent. In particular, suitable nanocontacts must provide low contact resistance and must be spatially uniform at the nanometer length scale. This requirement presents significant problems for nanocontacts based on any alloying process. For instance, in compound semiconductor devices based on GaAs, conventional contacts such as alloyed Au/Ge/Ni on n-type layers are spatially nonuniform and also consume a significant surface layer in order to provide suitably low specific contact resistance.[69] In this regard, uniform nonalloyed contacts are desired on a nanometer scale device. Patkar, et al.[68] have reported that nonalloyed contacts employing LTG:GaAs surface layers can provide specific contact resistance below 1×10^{-6} $\Omega\cdot\text{cm}^2$. Since these contacts will not suffer from the deep interface and spatially nonuniform alloying found in Au/Ge/Ni contacts, they are appropriate for nanometer scale device application. Furthermore, LTG:GaAs has slower oxidation rate (a few hours) than conventional GaAs (a few seconds) due to the relatively low concentration of minority carrier holes in the surface layer arising from the small minority carrier lifetime in LTG:GaAs material.[65,64] Therefore, LTG:GaAs material can be a proper material for nanometer scale device applications since Si and GaAs are rapidly oxidizing in air and this oxide causes nonuniform electric contacts.

The main goal of this thesis is the study of nanometer scale ohmic contacts. Controlled-geometry nanocontacts were formed by depositing Au clusters having diameters of 4 nm on LTG:GaAs and were characterized using STM spectroscopic techniques. A XYL SAM was employed on LTG:GaAs. This molecular layer forms an effective organic metal/semiconductor interface and provides both a robust mechanical tethering and a strong electronic coupling between the Au clusters and the LTG:GaAs surface. The Au clusters were encapsulated with DDT before deposition on the XYL-coated LTG:GaAs to prevent agglomeration of clusters. STM I-V data measured over nanocontacts exhibited an ohmic behavior with a significant enhancement in the conduction for low bias voltages compared to I-V data over the XYL-coated LTG:GaAs substrate, regardless of the dopant type of LTG:GaAs cap layer with good repeatability between various clusters distributed across the surface. When an undoped LTG:GaAs cap layer was used for nanocontacts, a specific contact resistance of 1×10^{-6} Ω·cm^2 and a current density of 1×10^{6} A/cm^2 were measured from STM.[78] For the case of nanocontacts using a Be-doped LTG:GaAs cap layer, the corresponding values were 1×10^{-7} Ω·cm^2 and 1×10^{7} A/cm^2, respectively.[79] The ohmic nanocontact is mainly due to the sequential tunneling through the XYL layer and the LTG:GaAs layer while a midgap band of defect states (midgap states) in the LTG:GaAs layer assists conduction as if it effectively reduces the barrier width. Improved surface stability as evidenced by a lower oxidation rate and conduction through the large amount of the midgap states distributed around the Fermi level in Be-doped LTG:GaAs provide a natural explanation for the higher quality ohmic contact properties of the nanocontact to the Be-doped LTG:GaAs cap layer.[79]

In this chapter, the STM experimental data on the nanocontact structure (Au cluster/XYL/LTG:GaAs) are presented. The ohmic nanocontact mechanism is discussed in the next chapter.

6.2 Au Nanoclusters

Nanometer size single crystal Au clusters are synthesized using an aerosol reactor known as a Multiple Expansion Cluster Source (MECS) in School of Chemical Engineering, Purdue University. A schematic of the MECS is shown in Fig. 6.1. Clusters with controlled diameters in the range of 2-20 nm can be synthesized in the MECS; the clusters used in this study are $\sim$ 4 nm in diameter. In the MECS, bare Au clusters are nucleated, grown, and annealed in an inert gas (he-

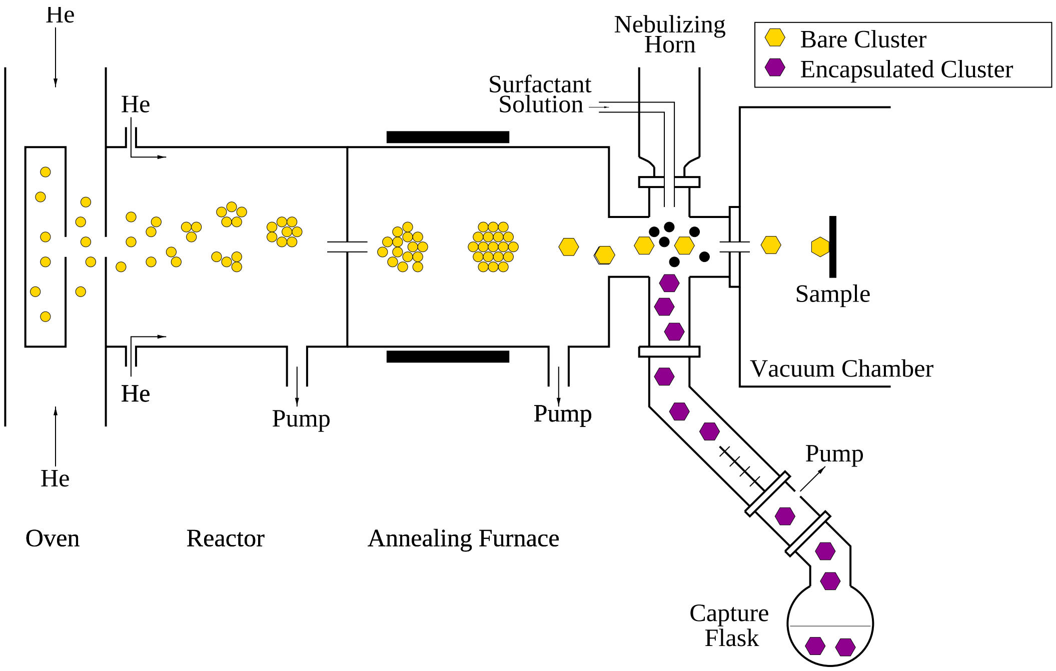


Figure 6.1

A schematic of the Multiple Expansion Cluster Source (MECS).

lium or argon) at reduced pressures. Each cluster is a fcc crystal, faceted in the shape of a truncated octahedron.[80] The bare Au clusters are encapsulated and protected from agglomeration by spraying a surfactant (e.g. DDT) solution into the aerosol flow downstream of the MECS. Detailed descriptions of the MECS can be found elsewhere.[81,82] The DDT encapsulated Au nanoclusters are soluble and form stable colloidal solutions in many nonpolar organic solvents, such as hexane, heptane, chloroform, mesitylene, etc. These encapsulated Au nanoclusters behave like simple chemical compounds; they can be precipitated, re-dissolved, and chromatographically separated without any apparent damage.[83] Compared to various liquid phase synthesis methods,[83,84] this aerosol synthesis has the following advantages: (i) the clusters are synthesized and annealed at very high temperatures so that each cluster is a well-faceted fcc single crystal; (ii) the clusters are charge neutral, which eliminates potential offset charge problems; (iii) both bare and encapsulated nanoclusters can be obtained, enabling studies on the effects of encapsulation on the crystal structure and other properties of the nanoclusters; (iv) the encapsulant can be displaced by a linking molecule in order to control the structural and electronic properties of the cluster networks.[18] (Au clusters were produced using MECS by Jia Liu.)

6.3 Nanocontact Structure: Au Nanocluster/XYL/LTG:GaAs

Fabrication of the nanocontact structure (Au cluster/XYL/LTG:GaAs) is schematically illustrated in Fig. 6.2. XYL can be used to tether the Au clusters

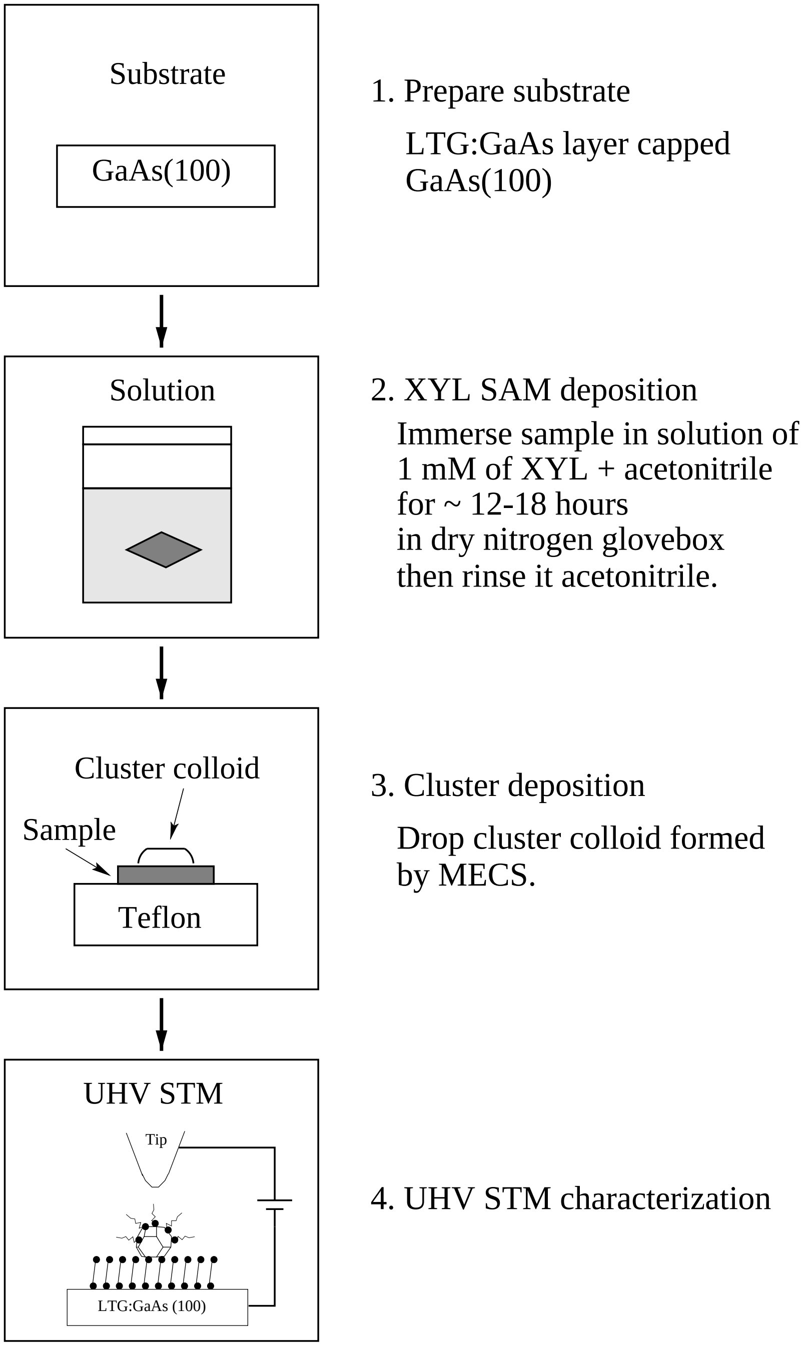


Figure 6.2

A schematic illustrating the fabrication procedure of the nanocontact structure: Au cluster/XYL/LTG:GaAs.

on the LTG:GaAs substrate because the thiol group at each end of XYL can bond effectively both to the LTG:GaAs and the faceted surface of Au cluster. Fig. 6.3 is a schematic illustrating STM operation on the nanocontact structure. The STM study over Au cluster/XYL/LTG:GaAs structure can be modeled by two resistors R_1 and R_2 connected in series where R_1 represents the equivalent resistance between the STM tip and Au cluster and R_2 represents the equivalent resistance between Au cluster and LTG:GaAs substrate through the interface monolayer of XYL. R_1 has an exponential dependence over z from Eq. (2.2) as

$$R_1 \propto e^{-2\kappa z} \quad , \tag{6.1}$$

where κ is given as Eq. (2.3). In principle, R_2 is the contact resistance of the Au cluster/XYL/LTG:GaAs, which is independent of z.[78]

Fig. 6.4 is a STM image of a Au nanocluster on XYL-coated LTG:GaAs. There is a cross sectional profile obtained along a line across the Au cluster in this figure. The apparent height and diameter of this Au cluster were found to be 3.3 nm and 14 nm, respectively. Thus, it can be concluded that the STM image of Au cluster is considerably broadened laterally by a tip convolution effect, but the apparent height is close to the real size of the cluster.

These Au clusters tend to orient with the hexagonal (111) facet parallel to the surface.[85] From top view, Au cluster looks like a hexagonal structure. Three facets of the hexagonal structure can be seen in a STM image in Fig. 6.5. To obtain a perfect hexagonal structure, a well defined and very sharp tip will be required.

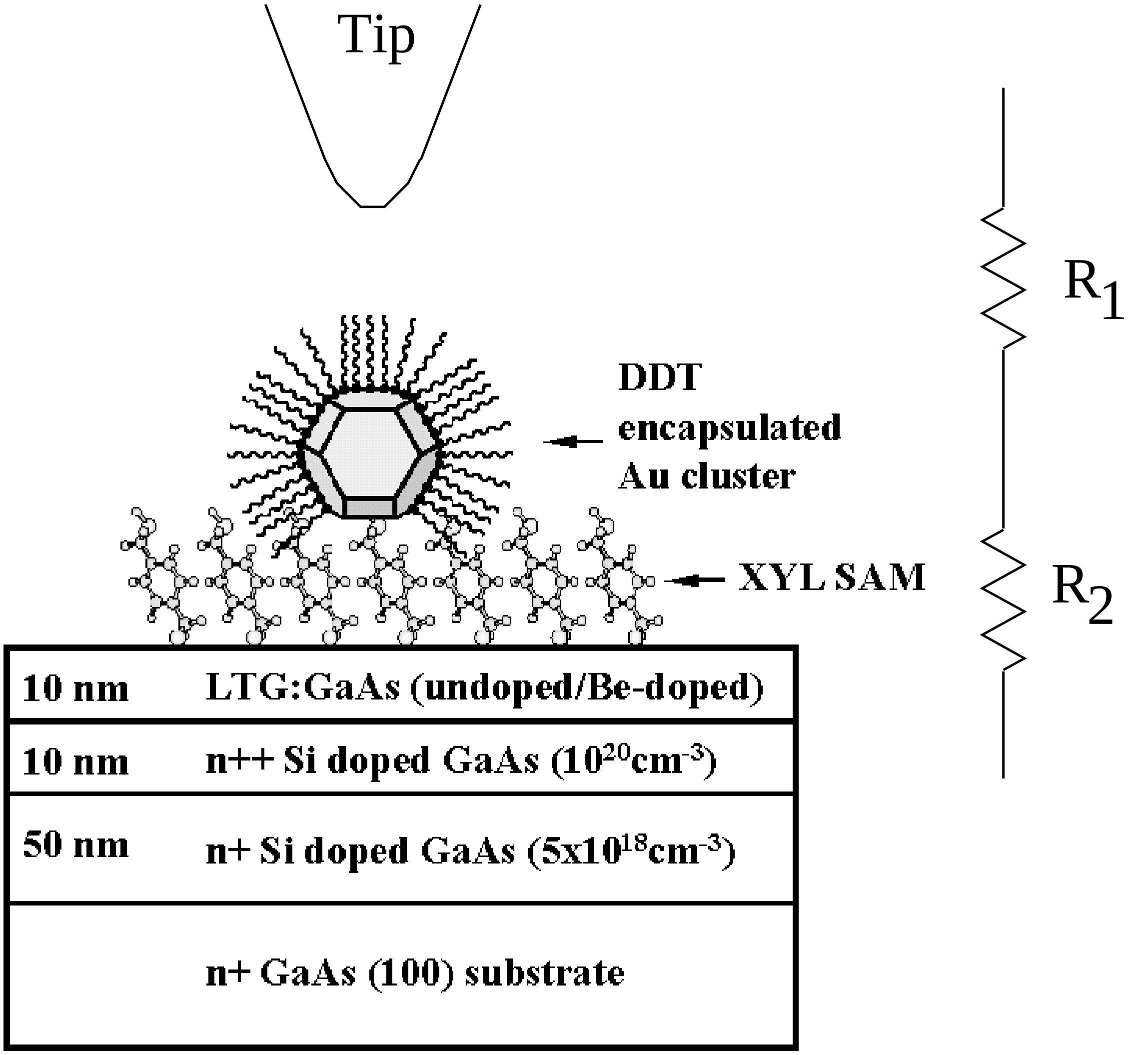


Figure 6.3

A Schematic illustrating STM operation on a Au cluster encapsulated with DDT, tethered on XYL-coated LTG:GaAs. This structure is modeled by two resistors R_1 and R_2 connected in series.

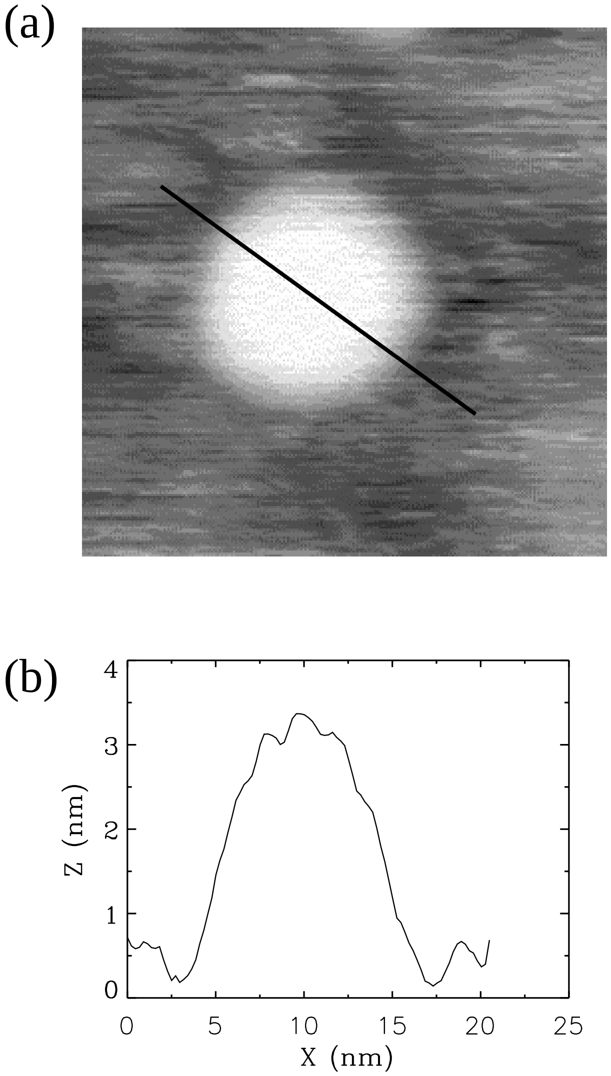


Figure 6.4

(a) A 25 nm × 25 nm UHV STM topographic image of a 4 nm diameter Au cluster tethered on XYL-coated undoped LTG:GaAs, acquired with $I_{set} = 1.0$ nA and V_{set} = -1.0 V. (b) A cross sectional profile obtained along a line across the Au cluster.

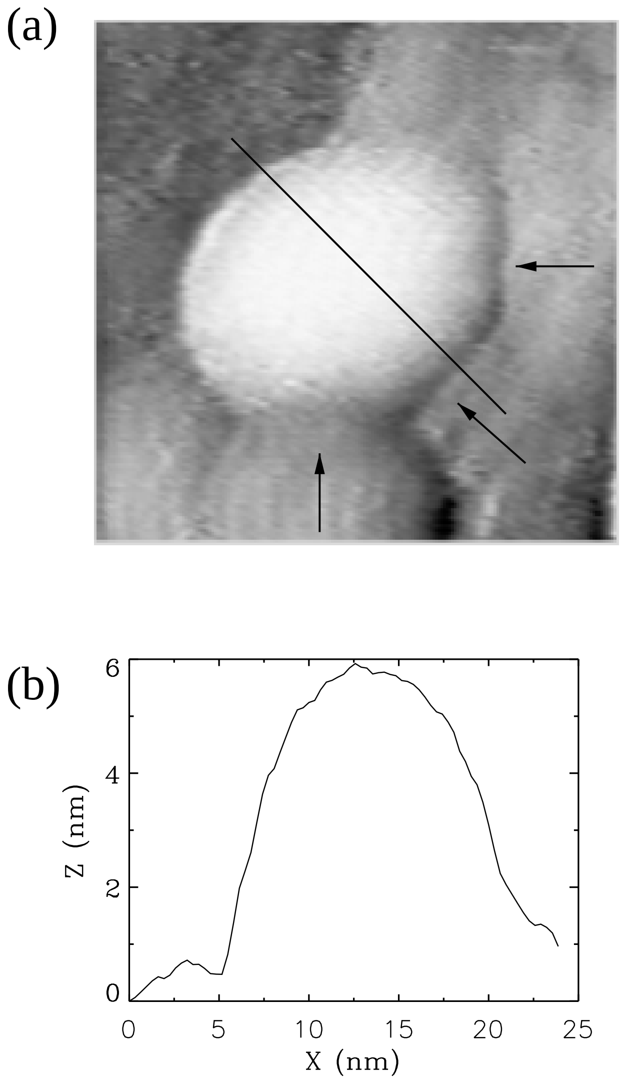


Figure 6.5

(a) A 30 nm × 30 nm filtered UHV STM topographic image of a 4 nm diameter Au cluster tethered on XYL-coated undoped LTG:GaAs, acquired with I_{set} = 0.7 nA and V_{set} = -1.0 V. The Au cluster shows three facets of the hexagonal structure indicated by arrows. (b) A cross sectional profile obtained along a line across the Au cluster.

Au clusters are encapsulated with DDT to prevent agglomeration of each other. Fig. 6.6 shows STM images of structures due to DDT (indicated as dots) covering around Au clusters when STM tip is scanned over a Au cluster far enough above it not to damage DDT molecules. STM images on a bare Au cluster without DDT molecules will not show this kind of structure.

The stability of Au cluster was studied by performing 100 consecutive imaging scans over an 80 minutes period of time. Two STM images in Fig. 6.7 are the first and last image out of 100 images of the same Au cluster. While imaging, I_{set} and V_{set} were 0.5 nA and -1.0 V, respectively. The Au cluster was observed to remain stable and didn't show any damage due to the scanning conditions employed. Therefore, it is concluded that these Au clusters are well tethered on LTG:GaAs with XYL molecules. A similar conclusion was reported in previous study when Au clusters were well tethered by XYL to a flat gold substrate.[5]

During 80 minutes imaging, the average thermal drift rate of x and y piezoelectric scanners were found to be 0.4 nm/min and 1.8 nm/min, respectively. The drift rates approached 0.2 nm/min and 0.9 nm/min for the x and y piezoelectric scanners, respectively after 80 minutes. This should be compared to time interval required to obtain a complete set of I-V data which is less than 1 s, therefore it is safe to say that STM tip is not moved away from a Au cluster when I-V is attempted at the center of cluster.

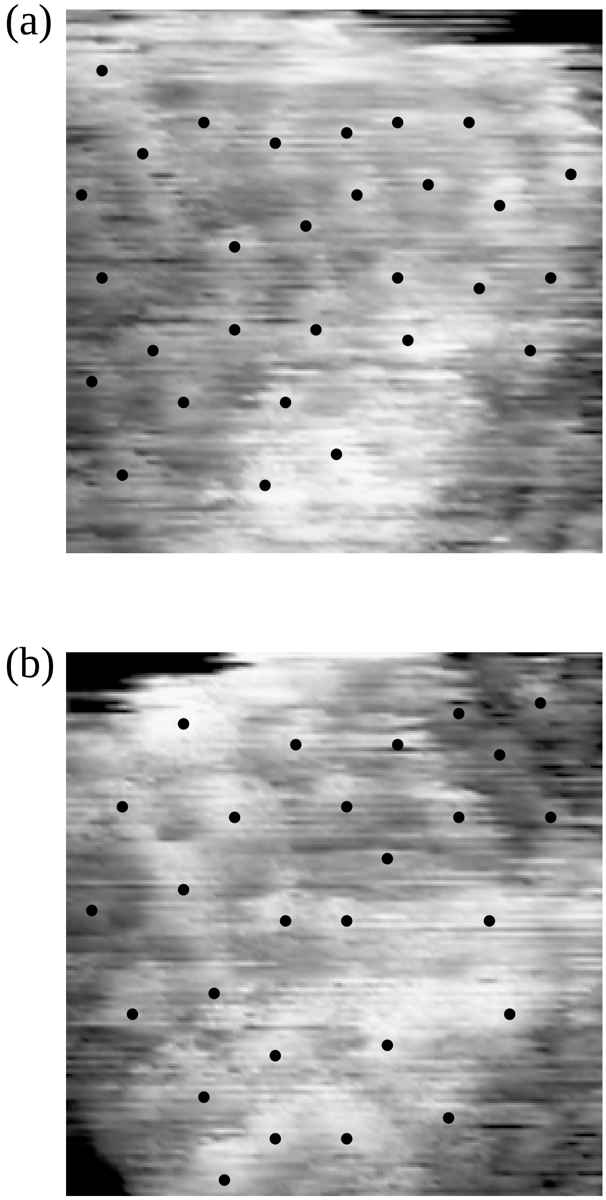


Figure 6.6

(a) A 6.3 nm × 6.3 nm UHV STM image on top of a Au cluster on XYL-coated Be-doped LTG:GaAs, acquired with I_{set} = 170 pA and V_{set} = -1.5 V. (b) A 7.0 nm × 7.0 nm UHV STM image on top of a Au cluster on the same sample. If the structures are due to DDT covering around Au clusters indicated as dots, then these structures are not well-defined hexagonal close-packed pattern.

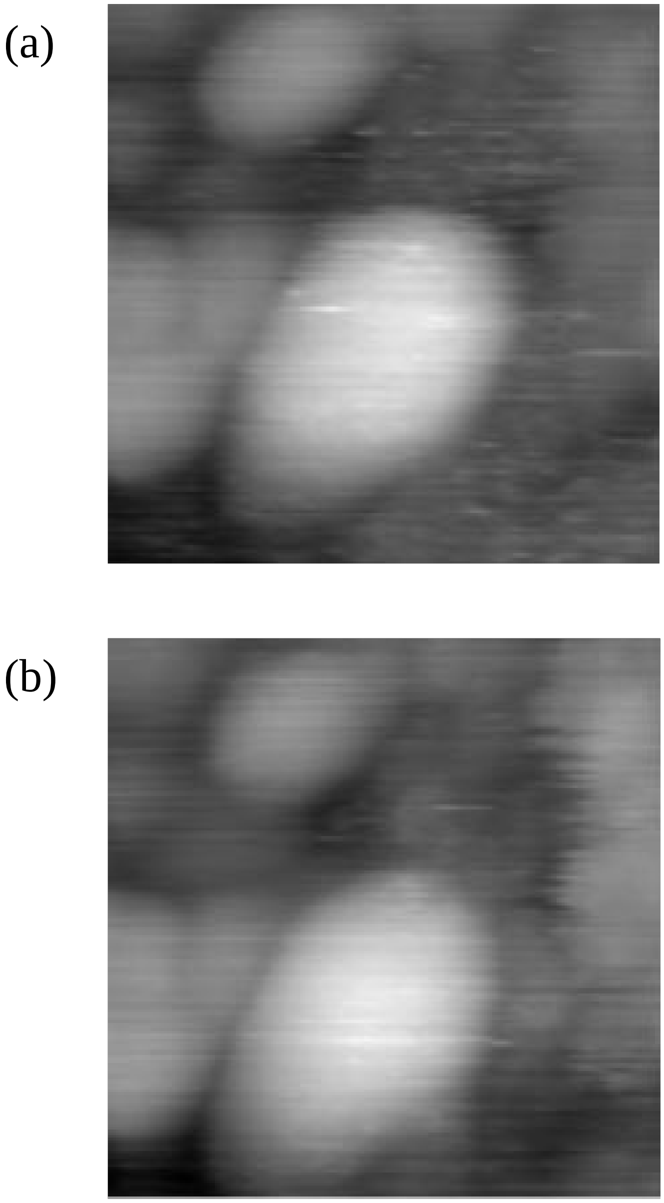


Figure 6.7

30 nm × 30 nm UHV STM topographic images of a Au cluster on XYL-coated undoped LTG:GaAs, acquired with I_{set} = 0.5 nA and V_{set} = -1.0 V in time sequence. Images (a) and (b) are the first and the last image of 100 consecutive images over 80 minutes. This implies that the Au cluster is well tethered on XYL-coated LTG:GaAs.

6.4 Ohmic Nanocontact: STM *I*-*V* Study

The Au nanocluster/XYL/LTG:GaAs structure was characterized in a similar way to the as-grown LTG:GaAs and SAM-coated LTG:GaAs samples discussed in the previous chapter. *I*-*V* measurements were performed over a Au cluster and substrate (XYL-coated LTG:GaAs). An ohmic contact behavior (linear *I*-*V*) was observed over Au cluster. Fig. 6.8 shows representative *I*-*V* data for cases where the STM tip was positioned over a Au nanocluster at various tip positions which were determined by V_{set} of -0.2 V (solid), -0.6 V (dotted), -1.0 V (dashed), -1.5 V (dash dotted), and -2.0 V (long dashed) with a fixed I_{set} = 0.8 nA. A smaller V_{set} represents a closer tip position over the surface of the sample in this plot. All the *I*-*V* curves show an ohmic behavior regardless of the tip sample separation. When the *I*-*V* measurement was performed over the substrate with the same measurement conditions, the data showed a bandgap feature of LTG:GaAs, as shown in Fig. 6.9. Therefore, when *I*-*V* was measured over a Au cluster, the data exhibited an ohmic behavior as if the conduction is significantly enhanced for low bias voltages compared to *I*-*V* data over the XYL-coated substrate. This kind of ohmic behavior was observed with good repeatability between various clusters distributed across the surface. True ohmic contact would exhibit a straight line *I*-*V* characteristic with a low value of resistance. But an ohmic contact does not necessarily require a linear *I*-*V* characteristics provided its resistance is very small compared with the resistance of bulk or active region of device.[86,87] Coulomb blockade effects, observed in earlier studies involving ~ 1 nm diameter Au cluster on Au substrate,[5] are not expected to occur here because of the relatively large size of the Au clusters employed.

The above results (ohmic I-V) imply that Au nanoclusters may be used as nanometer size ohmic contacts on GaAs. However, the linear I-V data does not provide the actual contact resistance R_2. For example, if the contact resistance R_2 is a low resistance ohmic contact, then the linear I-V data is mainly due to R_1 since the I-V measures the total resistance $R_{total} = R_1 + R_2$ and R_1 is much larger than R_2 in the STM I-V measurement in a low-current regime ($\sim$ nA range). In this case, only a small fraction of the applied voltage between tip and sample will be dropped across the nanocontact interface (Au cluster/XYL/GaAs) dependent on the ratio of R_2/R_{total} (see Fig. 6.3). This ratio in the low-current regime I-V is found to be around 0.01 since $R_{total} \simeq 1$ V/1 nA = 1 GΩ and $R_2 = \rho_c$/contact area $\simeq 10$ MΩ ($\rho_c \sim 10^{-6}$ Ω·cm^2 from Table. 6.2 and the contact area is the area of the cluster facet $\sim 10^{-13}$ cm^2). It means that only a small fraction $\sim$ 0.01 V of the applied voltage 1 V between tip and sample is dropped across the nanocontact interface and most amount of the applied voltage is dropped across R_1 component (tip-cluster vacuum gap). The linearity I-V in the low-current regime is hence due to R_1, however the linearity is consistent with the expectation that R_2 is a low resistance ohmic contact. In order to probe the nanocontact interface, performing I-V with a significant amount of the applied voltage dropped across the nanocontact interface and measuring R_2 are required, which is possible by bringing the STM tip close to Au cluster in “near contact mode STM”.

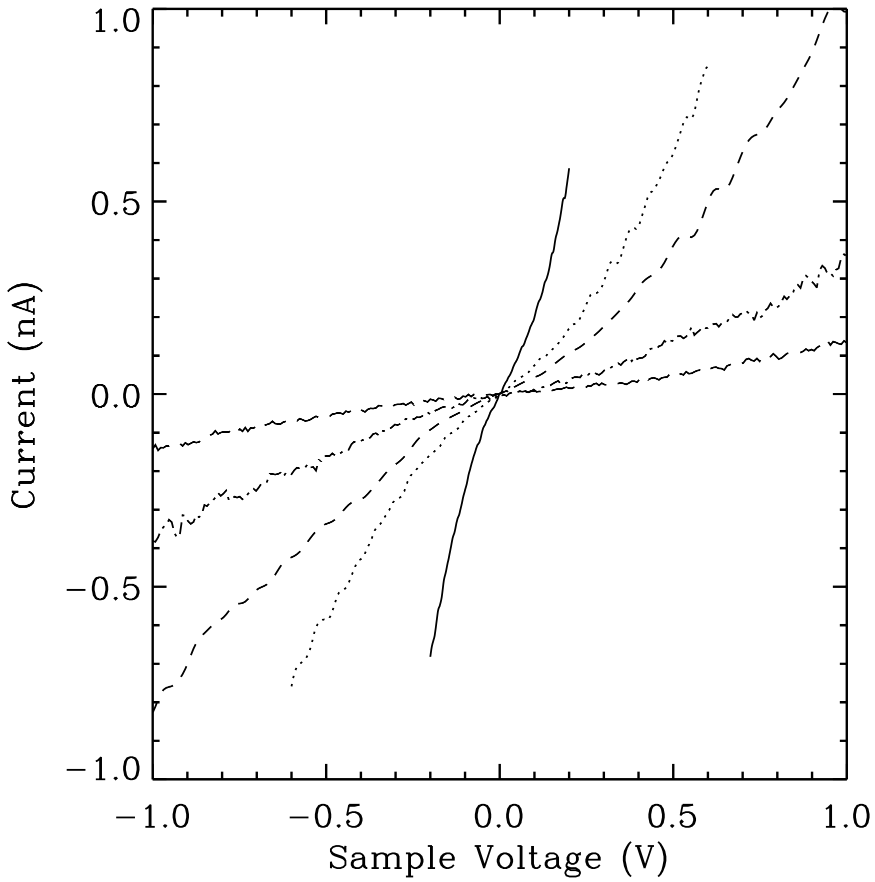


Figure 6.8

I-*V* data measured on a Au cluster tethered on XYL-coated undoped LTG:GaAs. The conditions of *I*-*V* measurement were 0.8 nA for I_{set} and -0.2 V (solid), -0.6 V (dotted), -1.0 V (dashed), -1.5 V (dash dotted), and -2.0 V (long dashed) for V_{set}. A smaller V_{set} represents a closer tip position over the surface of the sample. All the *I*-*V* data show an ohmic behavior.

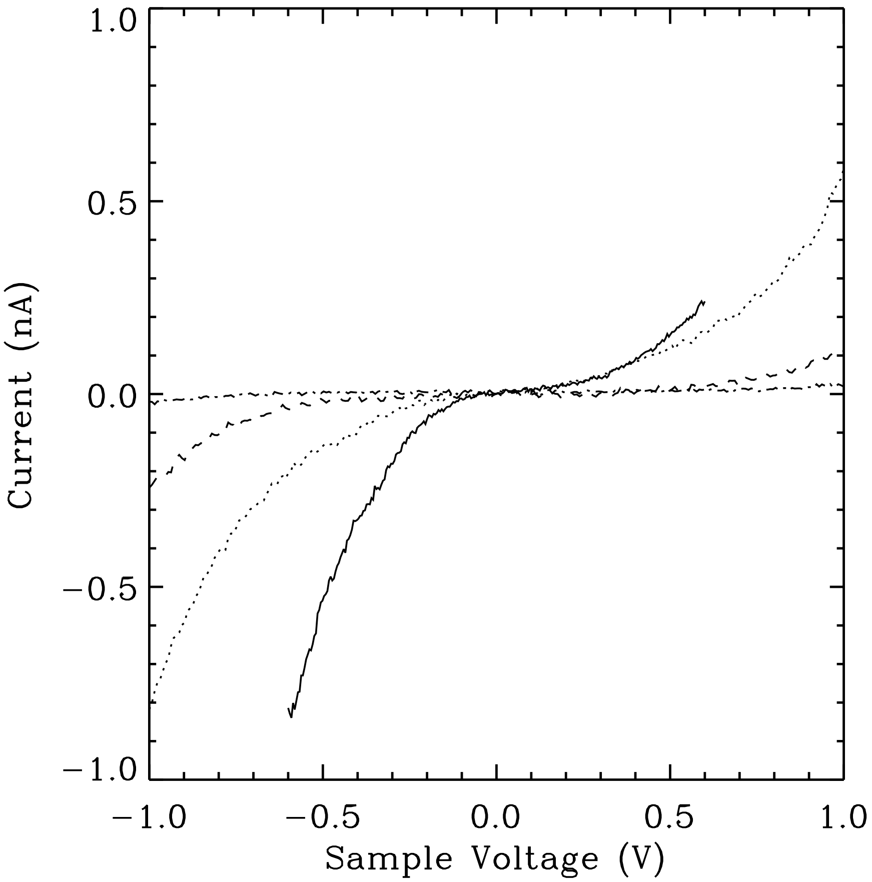


Figure 6.9

I-*V* data measured on the substrate (XYL/LTG:GaAs). The conditions of *I*-*V* measurement were 0.8 nA for I_{set} and -0.6 V (solid), -1.0 V (dotted), -1.5 V (dashed), and -2.0 V (dash dotted) for V_{set}. A smaller V_{set} represents a closer tip position over the surface of the sample. All the *I*-*V* data show an energy bandgap.

The non-linear behavior *I-V* over the substrate (Fig. 6.9) can be explained by the fact that the STM tip probes the electronic states of XYL/LTG:GaAs. The non-linearity in *I-V* on XYL/LTG:GaAs is due to the bandgap features of XYL and LTG:GaAs. It is similar to the studies on XYL/Au by STM, however in this case only XYL has the bandgap feature.[88]

The ohmic behavior was also observed using Be-doped LTG:GaAs cap layer sample. Fig. 6.10 shows a series of measured *I-V* data for cases where the STM tip was positioned over a Au cluster (solid curves C, D) and over the XYL-coated Be-doped LTG:GaAs surface (dashed curves A, B). Therefore, the ohmic nanocontact behavior does not depend on the dopant type of LTG:GaAs cap layer.

In order to make a significant fraction of the applied voltage dropped across the nanocontact structure, *I-V* was performed in a high-current regime ($\sim$ 100 nA). In this way, the STM tip is brought close to Au cluster and the ratio R_2/R_{total} becomes significant enough. The ohmic behavior is found to persist to higher tunnel currents when the tip is positioned over a Au cluster, as shown in Fig. 6.11. The solid curves correspond to a nanocontact with a Be-doped LTG:GaAs cap layer and the dashed curves correspond to a nanocontact with an undoped LTG:GaAs cap layer. A larger I_{set} represents a closer tip position to the sample. When a nanocontact structure with an undoped LTG:GaAs cap layer is probed, ohmic *I-V* characteristics were observed up to $\sim$ 30 nA. When *I-V* measurements were attempted at larger current levels, the STM tip was observed to dislodge the Au cluster. For these high currents, the STM tip comes so close to the cluster that

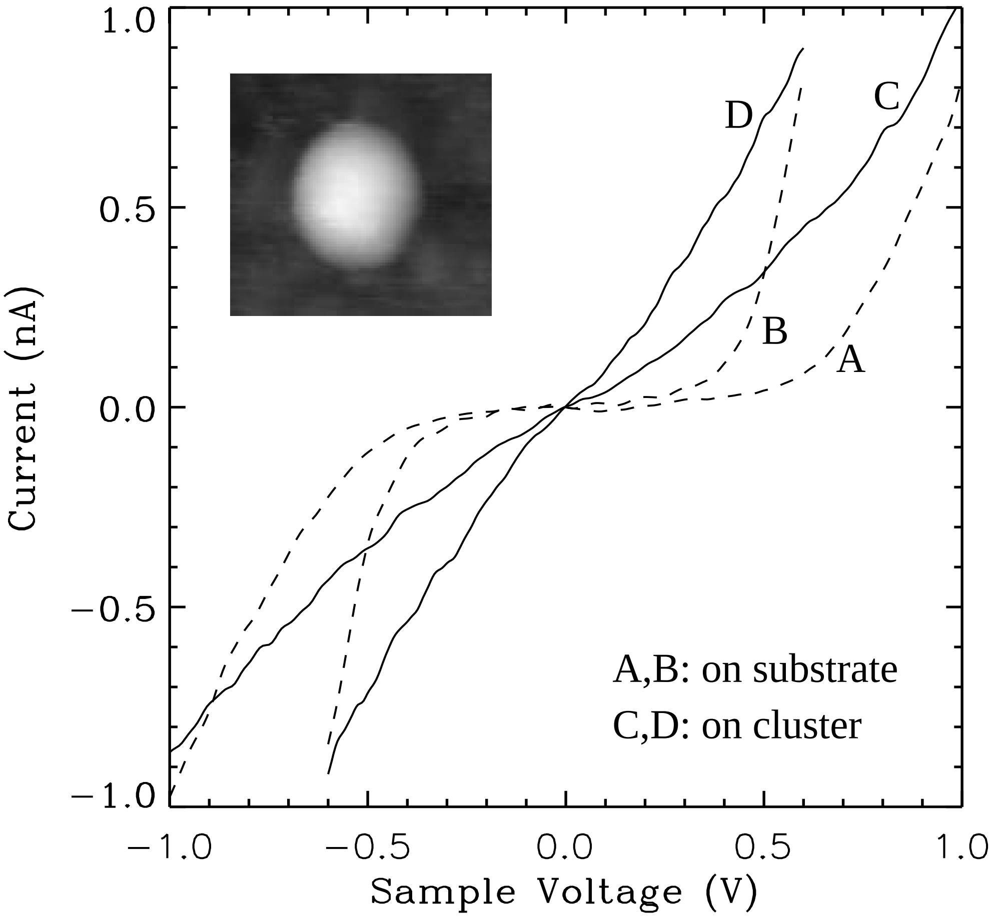


Figure 6.10

I-V data taken with the tip positioned over XYL-coated Be-doped LTG:GaAs (dashed) and over a Au cluster (solid) with 0.8 nA for I_{set} and -1.0 V (A and C), -0.6 V (B and D) for V_{set}. Inset picture is a 20 nm × 20 nm UHV STM topographic image of a Au cluster tethered on the XYL-coated Be-doped LTG:GaAs, acquired with I_{set} = 1.0 nA and V_{set} = -1.0 V.

it mechanically damages the nanocontact. For the case of a nanocontact with a Be-doped LTG:GaAs cap layer, the ohmic behavior persists to even higher tunnel currents (up to 200 nA) without damaging the Au cluster. These *I*-*V* curves in the high-current regime provide a more direct evidence for the ohmic contact. For example, from the *I*-*V* data over the nanocontact on the undoped LTG:GaAs (as dashed curve in Fig. 6.11), the ratio R_2/R_{total} is found to be around 0.2 since $R_{total} \simeq 1$ V/20 nA = 50 MΩ and $R_2 \simeq 10$ MΩ. This indicates that a significant amount (~ 0.2 V) of the applied voltage (1 V) is dropped across the nanocontact structure and this amount of voltage (~ 0.2 V) is enough to characterize the nanocontact structure. Therefore, the contact structure of Au nanocluster/XYL/LTG:GaAs can be safely referred to as an ohmic contact at the nanometer scale.

Fig. 6.12 shows two STM images of Au clusters on XYL-coated undoped LTG:GaAs before and after several *I*-*V* measurements were performed over a Au cluster (marked with X) in the image (a) while STM tip is close to the cluster. This cluster disappeared in the image (b).

I-*V* characteristics measured on LTG:GaAs, XYL/LTG:GaAs, and Au cluster/XYL/LTG:GaAs are summarized in Table. 6.1. Ohmic contact performance in Au cluster/XTL/LTG:GaAs is discussed in the next section.

6.5 Specific Contact Resistance: STM *I*-*z* Study

To interpret ohmic contact properties on Au cluster/XYL/LTG:GaAs structure, it is necessary to determine specific contact resistance which is widely used

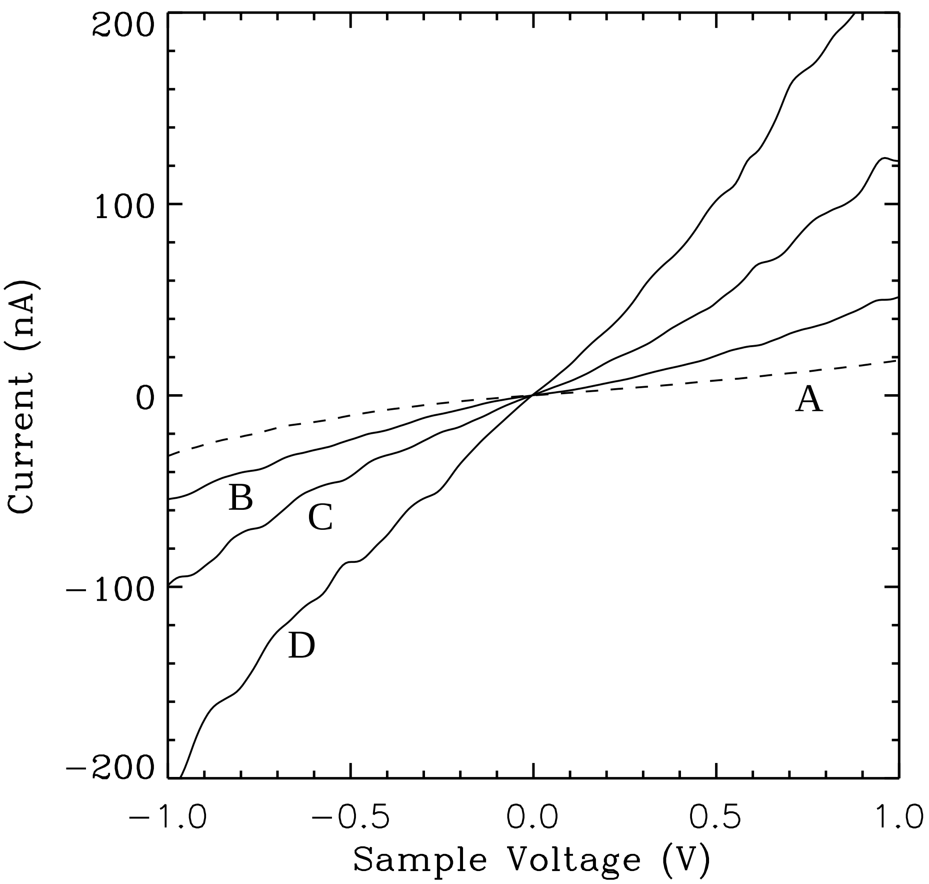


Figure 6.11

I-V data taken over a Au cluster tethered on undoped LTG:GaAs (dashed) with V_{set} = -1.0 V and I_{set} = 30 nA and on Be-doped LTG:GaAs (solid) with V_{set} = -1.0 V and I_{set} = 50 nA (B), 100 nA (C), and 200 nA (D). A larger I_{set} represents a closer tip position to the sample. This data indicates that the ohmic behavior on the nanocontact structures persists to higher tunnel currents.

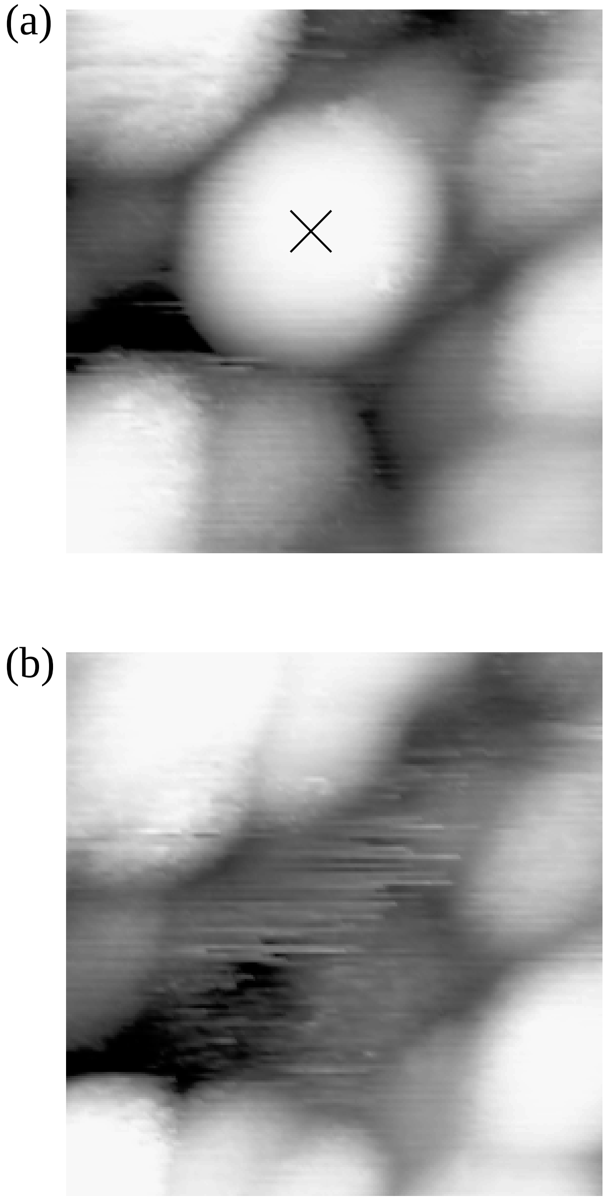


Figure 6.12

(a) A 25 nm × 25 nm UHV STM image of Au clusters on XYL-coated undoped LTG:GaAs, acquired with I_{set} = 1.0 nA and V_{set} = -1.0 V. (b) A UHV STM image on the same position as (a) after several I-V measurements were performed over a Au cluster (marked with X) in image (a) with a tip's close position determined by I_{set} = 1.0 nA and V_{set} = -10 mV. This cluster disappeared in this image.

Table 6.1

Summary of I-V characteristics measured on LTG:GaAs, XYL/LTG:GaAs, and Au cluster/XYL/LTG:GaAs.

	I-V shape	Apparent bandgap
I-V on GaAs	Non-ohmic behavior	1.4 eV [Ref. 89]
I-V on LTG:GaAs	Non-ohmic behavior	0.24 - 0.93 eV
I-V on XYL/LTG:GaAs	Non-ohmic behavior	0.53 - 1.2 eV
I-V on Au cluster/XYL/LTG:GaAs	Ohmic behavior	0 eV

as a parameter for ohmic contact performance. From the I-V curve of the closest tip position in Fig. 6.8 (I_{set} = 0.8 nA and V_{set} = -0.2 V), the resistance is found to be around 300 MΩ. The specific contact resistance ρ_c is defined by the resistance R_2 and the contact area $\mathcal{A}$ under the Au cluster as

$$\rho_c = R_2 \times \mathcal{A} \ , \tag{6.2}$$

where R_2 is the equivalent resistance between Au cluster and LTG:GaAs substrate through the interface monolayer of XYL, representing the contact resistance of the Au cluster/XYL/LTG:GaAs (see Fig. 6.3).

The ρ_c of this ohmic contact can be estimated due to the well-characterized, single crystalline Au clusters used in this study. From geometrical considerations, the area $\mathcal{A}$ of a Au(111) facet on a $\sim$ 4 nm high, truncated octahedral cluster is

$\sim 9 \times 10^{-14}$ cm^2. With this value for $\mathcal{A}$ and the measured resistance of 300 MΩ, the contact resistance ρ_c is calculated to be 3×10^{-5} Ω·cm^2. Actually this value provides an upper limit of the contact resistance of this nanocontact structure because the resistance of 300 MΩ measured from I-V data is a sum of R_1 and R_2, and only R_2 represents the contact resistance. Since the tunneling resistance between the tip and Au cluster (R_1) dominates in the measured resistance, the tip position should be very close to Au cluster to measure the realistic contact resistance on this structure. One problem with the I-V measurement at close tip position is that the STM tip often dislodges the Au cluster (see Fig. 6.12).

In order to determine ρ_c and set realistic limits on the maximum current capability of the nanocontact, a technique measuring I versus the tip-cluster spacing z (I-z) is preferable.[78] This technique is safer than a near contact I-V measurement because the time interval required to obtain a I-z data (a few msec) is much less than that required for a complete set of I-V data (a few sec) at the near contact. In the I-z measurement, the initial tip position is specified by I_{set} and V_{set}. Then the tip moves towards the sample by the distance of an assigned amount and moves back to the initial position while the resulting current is recorded. Fig. 6.13 is a plot of I-z measurement on a Au cluster tethered on XYL-coated undoped LTG:GaAs. In this plot, the initial height of the tip above the cluster was set by specifying an I_{set} = 0.5 nA and V_{set} = -1.0 V; negative values for the relative tip position represents tip motion towards the sample. In this case, the tip moved by 1.0 nm from the initial position. This I-z characteristic exhibits an exponential dependence of tunneling current on the gap distance between tip and Au cluster. From Eqs. (2.2) and (2.3), the apparent barrier height or work function (ϕ) can be measured from the I-z data and was found to be 0.73 eV. A low barrier height has been observed in a similar molecular system.[90] The measurement of a low barrier height is due to several barrier height lowering effects such as image force barrier lowering effect, molecular states-assisted tunneling, and tip sample interaction.[91,92]

As the tip moves closer to the cluster, the current is expected to saturate.[92–94] In the ideal case of metal-to-metal contact, the saturation current will represent a quantum conductance.[92] When saturation happens at near contact in I-z measurement, it is necessary to consider two issues.[95] First issue has to do with the instrument involved with the measurement. Olesen, et al.[96] has described a procedure of making the measurement where the voltage is measured directly across the tunnel junction. If the instrument used for the measurement has a comparable input impedance as the resistance of tip-sample junction, the actual voltage component applied only to the tip-sample junction will vary with the current because non-negligible voltage component will drop in the instrument. The STM system used for this study does not have this kind of problem because the instrument (Keithley 428 current amplifier) used in this study has the input impedance of 1 KΩ range which is negligible as compared with the resistance of the tip-sample junction (0.01-1 GΩ). Second issue is whether the tip and surface in the I-z plot are allowed to deform toward each other as the tip-surface distance becomes small. When any deformation happens, z-value of I-z data will not represent the real

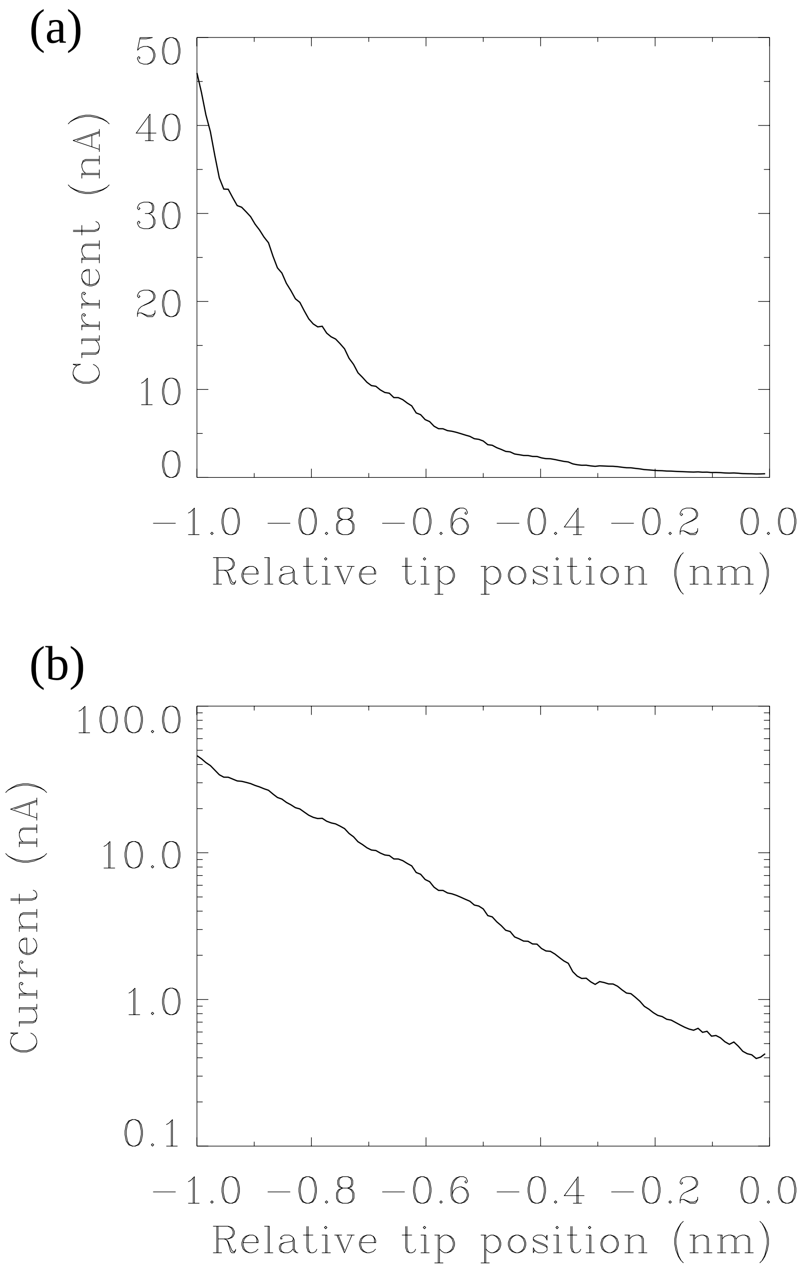


Figure 6.13

I-z plot in the linear scale (a) and the log scale (b) measured over a Au cluster tethered on XYL-coated undoped LTG:GaAs. Negative value of horizontal axis represents a relative tip motion towards the sample from an initial tip position (plotted at zero) determined by I_{set} = 0.5 nA and V_{set} = -1.0 V.

tip-sample gap distance and saturation current will be an artifact from this deformation. This kinds of tip and surface distortions may be a problem in the system involving “soft” materials. However, a previous study on a terphenylthiol SAM/Au[97] did not show a saturation current in I-z measurement when STM tip moved across the interface of vacuum gap and SAM layer, indicating that there is no deformation in this sample. Therefore, the saturation current in the nanocontact structure may not suffer from this issue.

When the tip contacts the cluster in the nanocontact structure, the tip-to-cluster resistance becomes negligible, so the current saturates at a value dictated by the resistance between the cluster and the semiconductor substrate (R_2). The latter resistance is the contact resistance for the nanocontact. Fig. 6.14 is the plot of I-z obtained with the tip positioned over a $\sim$ 4 nm high Au cluster on undoped LTG:GaAs (dotted) and on Be-doped LTG:GaAs (solid) which have been passivated by XYL layer. Data for the Be-doped sample was shifted by 0.5 nm to account for difference in initial heights due to different set conditions. When the tip moves by 1.5 nm for the nanocontact on undoped LTG:GaAs sample, the tunnel current increases exponentially with the gap distance for a relative tip displacement from the initial position by $\sim$ 1.0 nm, indicating that the resistance R_1 between tip and Au cluster is still dominant because R_1 has an exponential dependence over z.

As the tip moves closer to the sample, the current saturates and approaches an asymptotic value (saturation current) as indicated by the dashed line, at

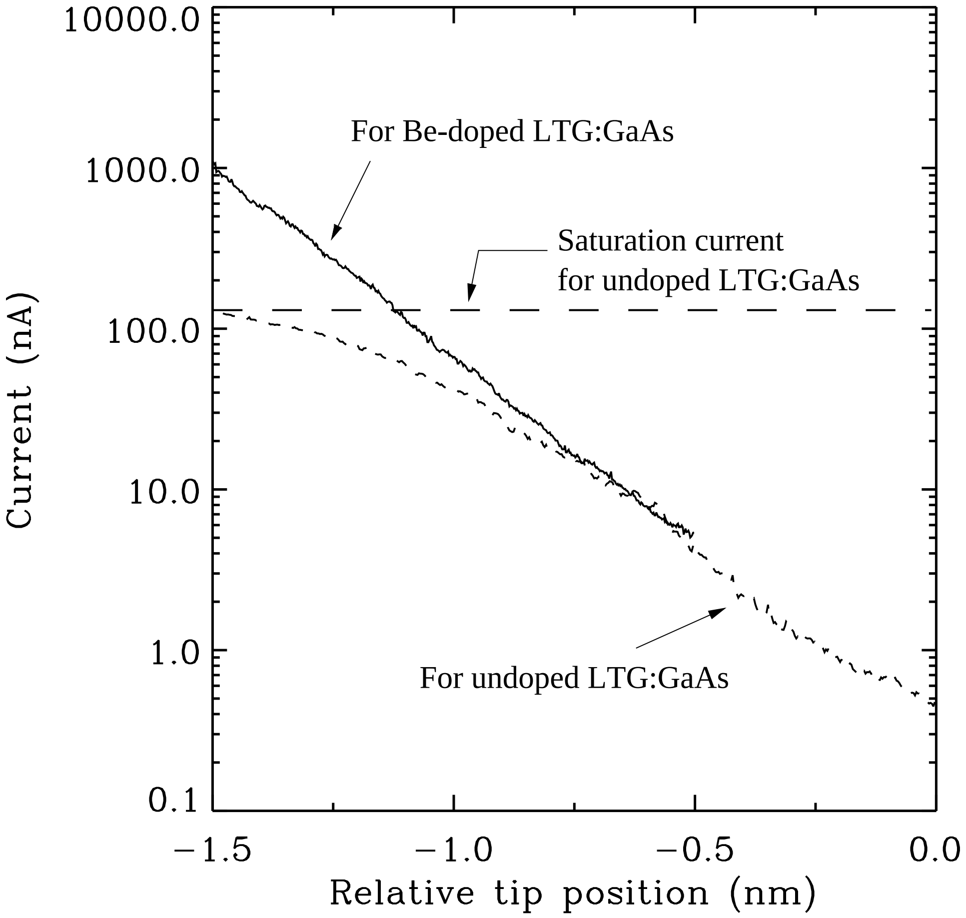


Figure 6.14

A log plot of I-z over a Au cluster tethered on undoped LTG:GaAs (dotted) and on Be-doped LTG:GaAs (solid) at a constant V_{set} = -1.0 V. The initial separation corresponding to I_{set} = 0.5 nA and 3.0 nA is plotted at zero and at -0.5 nm for undoped and Be-doped LTG:GaAs, respectively.

which point the measured resistance is dominated by R_2 between the cluster and LTG:GaAs, so that $R_2 \approx R_{total} = R_1 + R_2$. This saturation current of $\sim$ 100 nA with area $\mathcal{A}$ can be used to estimate the contact resistance ρ_c:

$$\rho_c \approx R_{total}\, \mathcal{A} = (V/I)\, \mathcal{A} \approx (1.0 \text{ V}/100 \text{ nA})\ (1 \times 10^{-13} \text{ cm}^2)$$

$$= 1 \times 10^{-6}\ \Omega{\cdot}\text{cm}^2\ .$$

The current density through the Au cluster can be calculated with the saturation current and the area $\mathcal{A}$ and was found to be 1×10^{6} A/cm^2.

Compared with undoped LTG:GaAs, a Be-doped LTG:GaAs cap layer (solid curve in Fig. 6.14) did not show the saturation effect. Instead, the I-z relationship remained roughly linear up to 1000 nA, the measurement limit of the STM system. This means that the tip is still not in near contact to the Au cluster. Using the maximum current (1000 nA) for the Be-doped LTG:GaAs capped sample, an upper bound for ρ_c of $\sim 1 \times 10^{-7}$ $\Omega{\cdot}$cm^2 and a lower bound for J_{max} of $\sim 1 \times 10^{7}$ A/cm^2 were determined.

The reason why saturation happened only in the nanocontact on undoped LTG:GaAs can be qualitatively explained by comparing R_1 and R_2 as a function of the tip-sample distance (z), as shown in Fig. 6.15. In this plot, R_1 has an exponential dependence on z. R_2 is constant as z is varied. For the nanocontact on undoped LTG:GaAs ($\rho_c \sim 1 \times 10^{-6}$ $\Omega{\cdot}$cm^2), saturation happens at the tip's near contact to the cluster where R_1 is smaller than R_2. For the nanocontact on Be-doped LTG:GaAs ($\rho_c \sim 1 \times 10^{-7}$ $\Omega{\cdot}$cm^2), saturation does not happen at the tip's near contact to the cluster because R_1 is still bigger than R_2.

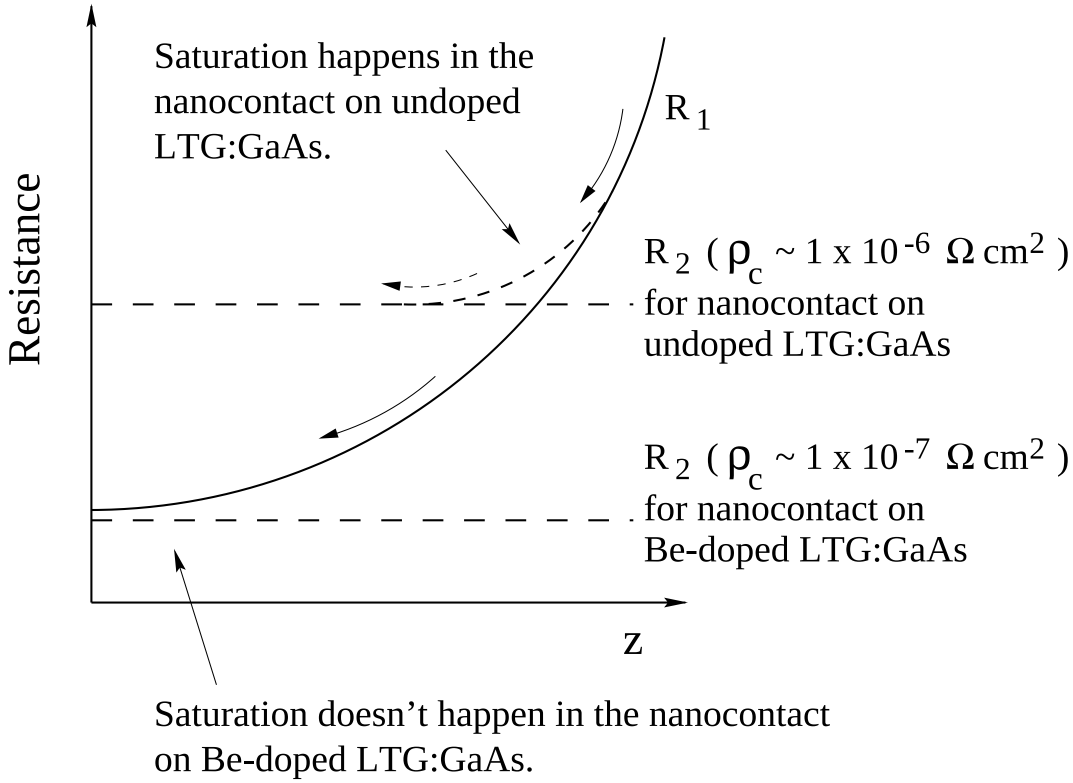


Figure 6.15

A schematic plot of resistance components (R_1 and R_2) versus tip-sample distance (z). R_1 has an exponential dependence on z and R_2 is constant over z (see Fig. 6.3 for R_1 and R_2). For the nanocontact on undoped LTG:GaAs ($\rho_c \sim 1\times10^{-6}$ $\Omega\cdot\mathrm{cm}^2$), saturation happens at the tip's near contact to the cluster where R_1 is smaller than R_2. For the nanocontact on Be-doped LTG:GaAs ($\rho_c \sim 1\times10^{-7}$ $\Omega\cdot\mathrm{cm}^2$), saturation does not happen at the tip's near contact to the cluster because R_1 is still bigger than R_2.

The I-z curve for the nanocontact on undoped LTG:GaAs in Fig. 6.14 (indicated as dotted curve) does not show a fully saturated behavior. The curve appears to increase even at the tip's closest position over the cluster (at -1.5 nm in this plot). Therefore, the estimate of ρ_c is not exact. More realistic value of ρ_c on undoped LTG:GaAs can be deduced from a constant fitting technique. Fig. 6.16 shows a measured resistance (R_{total}) versus relative tip position over the nanocontact on undoped LTG:GaAs (data from Fig. 6.14). Dashed curve in this plot is a calculated resistance (R_1) which is the measured resistance minus a fitting parameter for the contact resistance (R_2). Since R_1 has an exponential dependence on z, a log plot of R_1 versus z should be a straight line if a proper fitting parameter of the contact resistance is used. 6.5 ± 0.5 MΩ was used as the contact resistance for the best fitting to obtain a straight line. Using 6.5 MΩ for R_2 and Eq. (6.2), ρ_c can be determined as $\sim 7 \times 10^{-7}$ Ω·cm^2 for this nanocontact.

If a perfect XYL SAM is formed under Au cluster, 35 ± 5 XYL will contribute as current channels for the nanocontacts, because the faceted area of 4 nm Au cluster is $\sim$ 9 nm^2 and the area per XYL is $\sim$ 0.25 nm^2. A contact resistance per XYL molecule for the nanocontact on undoped LTG:GaAs can be determined from the fitting parameter of contact resistance $R_2 = 6.5 \pm 0.5$ MΩ and the number of XYL molecules under the cluster, and it was found as 230 ± 50 MΩ (6.5 MΩ $\times$ number of XYL molecule). But this value is dependent on the number of XYL under the cluster. It would be less than 230 MΩ if XYL SAM is not perfectly formed under the cluster. When XYL was used as a tether molecule of Au clusters

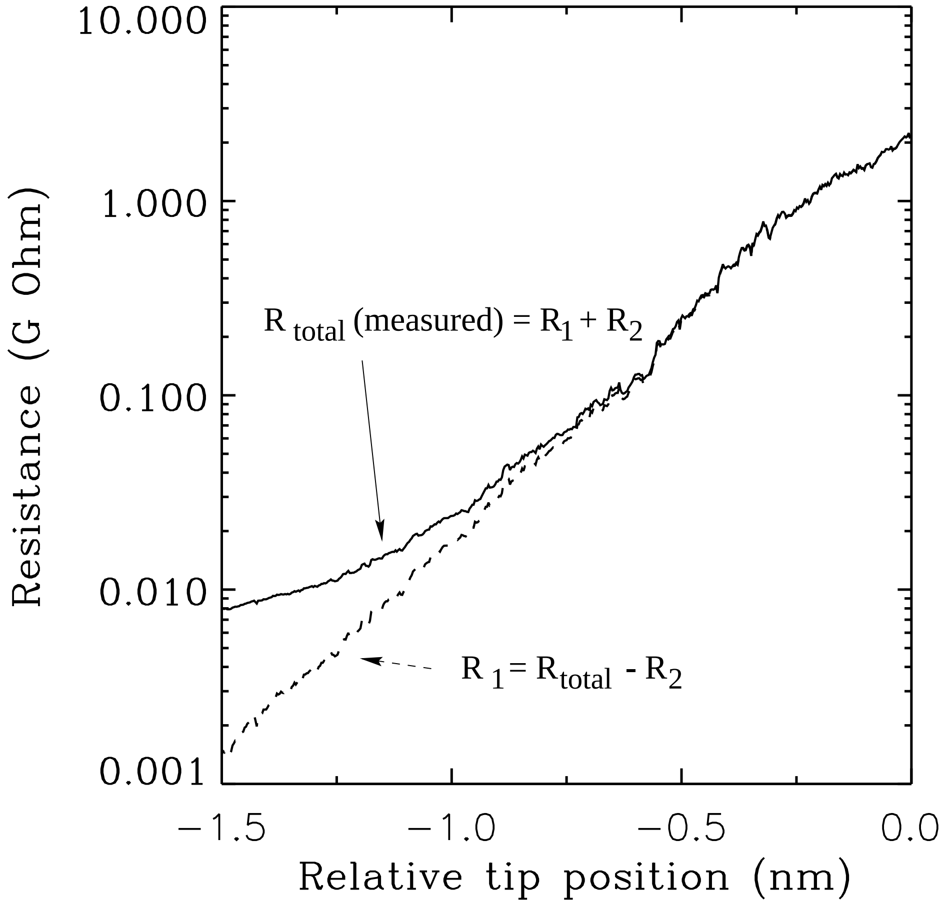


Figure 6.16

A log plot of measured resistance ($R_{total} = R_1 + R_2$, solid curve) versus relative tip position over the nanocontact on undoped LTG:GaAs. Dashed curve is a calculated resistance (R_1) which is the measured resistance minus a fitting parameter for the contact resistance (R_2). Since R_1 has an exponential dependence on z, log plot of R_1 versus z should be a straight line with a proper fitting parameter of the contact resistance. 6.5 MΩ was used as the contact resistance for the best fit.

Table 6.2

Summary of ohmic contact properties of the nanocontacts on undoped and Be-doped LTG:GaAs samples.

	Nanocontact on undoped LTG:GaAs	Nanocontact on Be-doped LTG:GaAs
Saturation current	$\sim$ 100 nA	$>$ 1000 nA
ρ_c	$\sim\ 7 \times 10^{-7}\ \Omega\cdot\text{cm}^2$	$\sim\ 1 \times 10^{-7}\ \Omega\cdot\text{cm}^2$
J_{max}	$\sim\ 1 \times 10^{6}\ \text{A/cm}^2$	$\sim\ 1 \times 10^{7}\ \text{A/cm}^2$
R/Molecule	230 ± 50 MΩ	< 35 MΩ

on Au(111) film, the resistance per XYL molecule was estimated to be roughly 9 MΩ.[98]

The ohmic contact properties such as specific contact resistance ρ_c and current density J_{max} for nanocontacts on undoped and Be-doped LTG:GaAs cap layer are summarized in Table 6.2. These results compare favorably to reported ρ_c values in the mid $10^{-7}\ \Omega\cdot\text{cm}^2$ range obtained from studies using 40 μm × 100 μm contact pads.[68]

7. NANOCONTACT MECHANISM

7.1 Metallic Nanoclusters on Semiconductors

In order to discuss the ohmic nanocontact mechanism in Au nanocluster/XYL/LTG:GaAs structures, it is necessary to examine what type of interfaces can be produced in metallic nanocluster on semiconductor surfaces.

Electronic properties of metallic nanoclusters on semiconductors depend on the metal comprising the cluster, the size of cluster, the semiconductor substrates, and the fabrication techniques. Until now, metal/semiconductor nanostructures fall into three broad categories: (i) single electron tunneling (SET) devices, (ii) nanoscale Schottky barriers, and (iii) nanoscale ohmic contacts. Generally a metallic cluster on a semiconductor surface will provide a metal-semiconductor (M-S) type interface. When the size of a cluster is reduced to a few nanometers, there can be additional effects due to size.

An example of a useful electronic effect related to size is the SET effect which has been observed in studies of Au clusters on p-Si(111),[99,100] Ag clusters on p-Si(100),[101] and Ag clusters on n-GaAs(110).[102] The size of cluster in these studies was determined from the height of cluster in STM topographic images since the lateral size of a cluster in a STM image is usually broadened by tip convolution effect. When the size of cluster is reduced to the nanometer scale, the capacitance of the structure can be low enough so that the single electron charging energy $e^2/2C$ can be large compared to the thermal energy k_BT (k_B is Boltzmann's constant) which is about 26 mV at room temperature. For asymmetric structures, this effect is observed as steps in an I-V curve or oscillations in dI/dV and is known as a Coulomb staircase. Also the tunneling probability is very small for voltages smaller than $e/2C$, resulting an energy gap in this voltage region. This phenomenon is referred to as Coulomb blockade. Typically single electron tunneling effects at room temperature can be observed in a cluster less than $\sim$ 3 nm in diameter.

Metallic clusters on semiconductors also produce a M-S interface. Depending on the respective work functions and other electronic properties, the structure could result in either a Schottky barrier or an ohmic contact structure. SET effects will not be expected when the size of the cluster is typically more than $\sim$ 3 nm. Nanoscale Schottky barriers were fabricated with Pt clusters on n-GaAs and n-InP,[103,104] Au clusters on n-Si(111),[105] and Cu clusters on TiO_2.[106] Stroscio, et al. observed metallicity within the bandgap of a nanoscale Schottky barrier structure with Fe clusters on GaAs(110).[107] In this case, the metallic behavior in STM I-V curve was attributed to metallic cluster-induced gap states.

As evidenced in the previous chapter, the Au cluster/XYL/LTG:GaAs nanostructures showed ohmic contact properties. In following sections, the mechanism of the nanoscale ohmic contact is discussed.

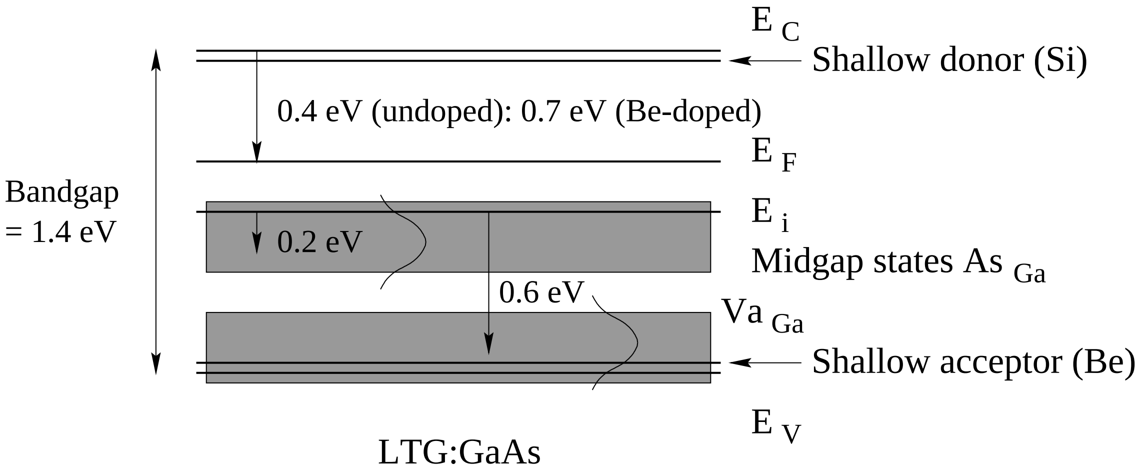


Figure 7.1

Energy band diagram of LTG:GaAs.

7.2 Mechanism of Large Area Ohmic Contact

As a starting point for modeling of the performance in the ohmic nanocontact structure, a quantitative conductance model for the large area ohmic contact (metal/LTG:GaAs) has recently been developed by Nien-Po Chen in Department of Physics, Purdue University. In what follows, the important findings of this conduction model are summarized in a qualitative way as described elsewhere.[108]

This analysis calculates the conduction band profile for the semiconductor structure using a Poisson equation solver (ADEPT),[109] and incorporates the characteristics of the LTG:GaAs defect states and Fermi statistics using parameters for the midgap and shallow acceptor states in the LTG:GaAs which are consistent with experimental observations as shown schematically in Fig. 7.1.

The calculated energy band profiles for the large area contact structures with Ti on 3 nm thick undoped LTG:GaAs layer are shown in Fig. 7.2 (See Appendix D for ADEPT simulation input file). The reference energy indicated by zero represents the vacuum level in these plots. Since the conduction band profile is reasonably approximated by a parabolic shape, the contact resistance can be calculated by applying expressions for uniformly doped Schottky contact with equivalent barrier heights and effective depletion depths.[108,110] This model adequately predicts experimental trends[68] for specific contact resistance (ρ_c) versus LTG:GaAs layer thickness and versus temperature. The surface barrier height (Φ_B) of oxidized undoped LTG:GaAs is the midgap value 0.7 eV, which would be expected if surface Fermi level pinning occurs at the midgap of LTG:GaAs,[27] as shown in Fig. 7.2 (a). Since the midgap surface pinning is associated with surface states arising from oxidation, a LTG:GaAs having Φ_B of 0.7 eV will have a less ohmic contact performance when a metal contact is made. On the other hand, when a metal contact is made on "fresh" LTG:GaAs before it is significantly oxidized, Φ_B is expected to be significantly reduced. Based on comparison between the experimental results[68] of ρ_c and the simulation analysis,[108] (i) Φ_B appears to be ~ 0.3 eV in the ohmic contact structure, well below midgap value of 0.7 eV and (ii) a high density of donors 1×10^{20} cm^{-3} above the bulk amphoteric limit 5×10^{18} cm^{-3} has been achieved in the n++ GaAs space charge region [Fig. 7.2 (b)]. This implies that the LTG:GaAs surface is not pinned at midgap, indicating a relatively low surface state density at the LTG:GaAs surface and therefore that the surface is not significantly oxidized.

It is typically not possible to achieve either of these effects (low barrier height and high donor density) in *ex-situ* contacts to n-type GaAs due to the surface Fermi level pinning associated with rapid surface oxidation and the bulk amphoteric doping limit in stoichiometric GaAs layers. The achievement of both effects in this structure is attributed to the passivation effects of the LTG:GaAs layer and to the associated Fermi level control.[79,108] The ability to achieve a donor density within the space charge region which is higher than the bulk amphoteric limit has been explained in terms of the control of Fermi level during the growth.[68]

It should be noted that the semiconductor heterostructure is typically exposed to air for prolonged periods (typically weeks) before contact processing, so a portion of the LTG:GaAs layer oxidizes during this period. Since this oxidation appears to cause midgap surface Fermi level pinning even in LTG:GaAs, the surface oxide must be stripped (with dilute HCl) shortly before contact metallization. The oxide strip restores the surface Fermi level to an unpinned state, with a re-oxidation time constant of several hours.

In the large area contact, the conduction mechanism is primarily tunneling (field-emission and/or thermionic field emission) from the metal into the n++ GaAs layer while conduction through the midgap band of defects states also plays a role.[108]

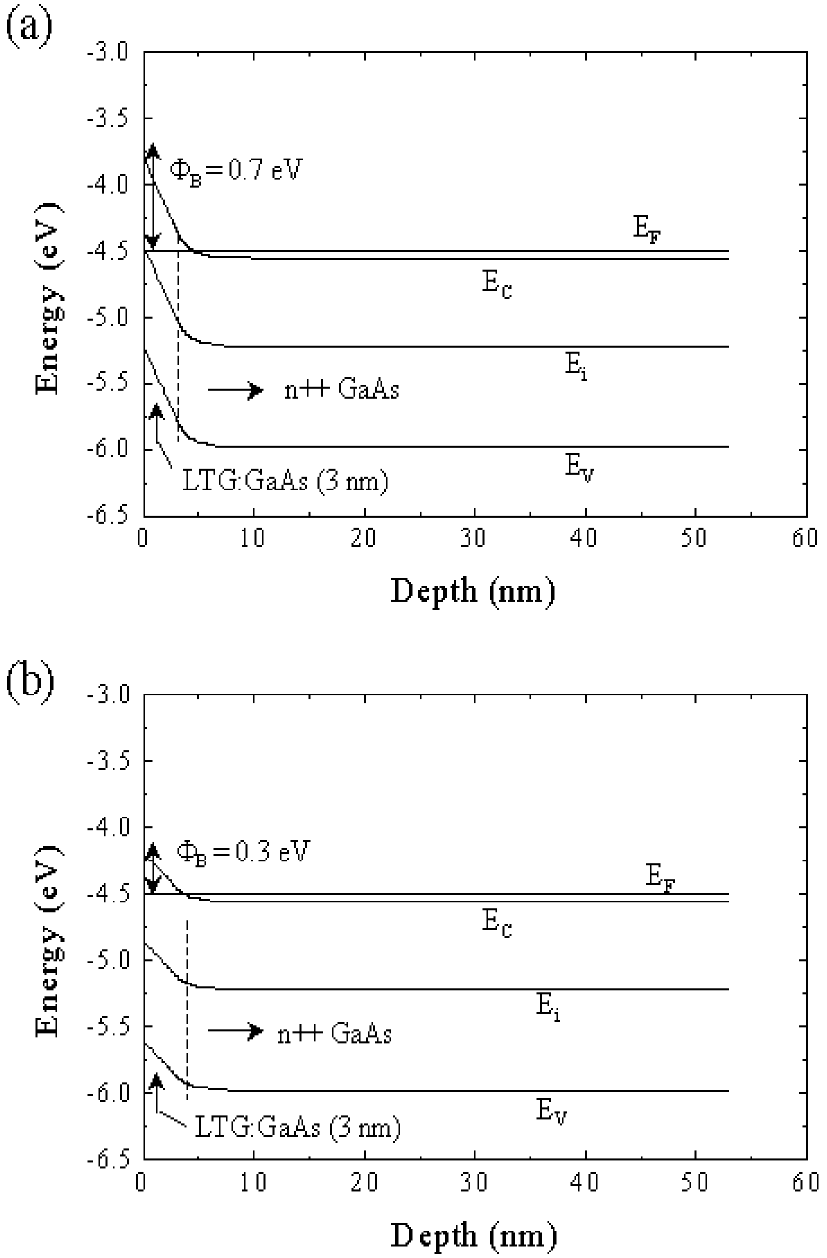


Figure 7.2

Calculated energy band profiles of (a) Ti/LTG:GaAs (oxidized, undoped) and (b) Ti/LTG:GaAs (unoxidized, undoped) ohmic contact layers. The reference energy indicated by zero represents the vacuum level.

7.3 Nanocontact vs Large Area Contact

For the nanocontact structure (Au cluster/XYL/LTG:GaAs), the conduction model in the previous section must be modified to incorporate the effects of the layer of XYL between the cluster and the LTG:GaAs surface. The structure is similar to a metal-insulator-semiconductor (M-I-S) interface. Qualitatively, the XYL layer can be described as a leaky dielectric. There are states associated with the molecular levels (HOMO and LUMO states). Generally, one of these two levels will be within 0.5-1 eV of the Fermi level when the molecules are sandwiched between two metallic electrodes [see Fig. 7.7 (a)]. Since the dielectric constant of this layer (~ 2) is considerably lower than that of GaAs (~ 13), a relatively large portion of the electrostatic potential difference between the metal cluster and the semiconductor bulk is dropped across the XYL layer.

There are several key differences between the large area contact structure and the nanocontact structure: (i) the nanocontact structure employs a thicker LTG:GaAs layer (10 nm) than the large area contact structure (<5 nm LTG:GaAs), which should diminish the ohmic contact properties from the large area conduction model; (ii) the work function of Au (~ 5.1 eV) is larger than that of the Ti metallization (~ 4.3 eV) used in the large area contact, which tends to raise the barrier heights in the M-I-S with respect to that of the M-S structure.

The calculated energy band profiles for the nanocontact structures are shown in Fig. 7.2 (See Appendix D for ADEPT simulation input file). LTG:GaAs with 8 nm thick layer was used for the calculation since a few nanometers of LTG:GaAs will

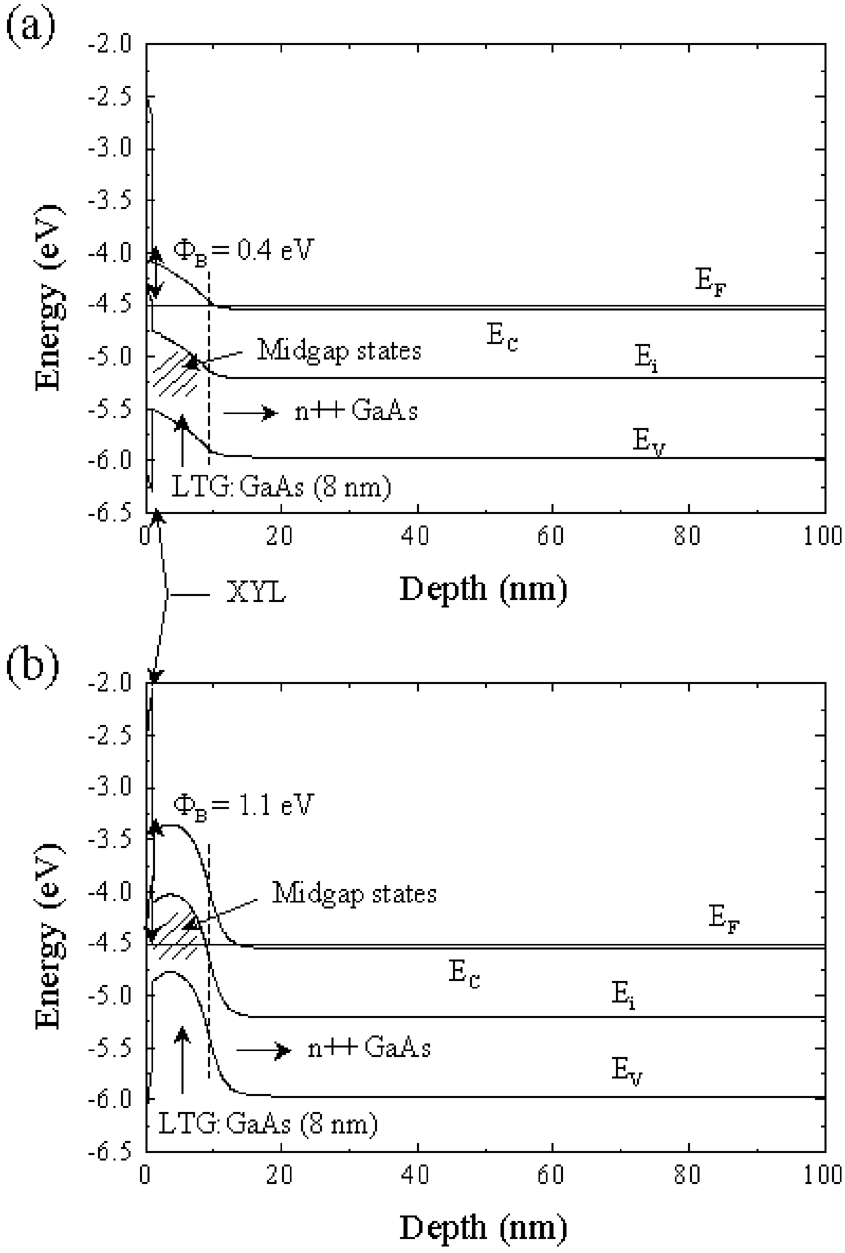


Figure 7.3

Calculated energy band profiles of (a) XYL/LTG:GaAs (undoped) and (b) XYL/LTG:GaAs (Be-doped) ohmic contact layers.

be removed during HCl etching before XYL deposition.[108] The conduction band profile of undoped LTG:GaAs and n++ GaAs layers in Fig. 7.3 (a) represents an approximately parabolic shape which looks similar to those in the large area contacts as shown in Fig. 7.2 (a) and (b). Therefore, ρ_c can be predicted in the same method that was used for the large area conduction model. Fig. 7.4 (a) shows a plot of calculated ρ_c versus work function of Au cluster tethered on undoped LTG:GaAs layer with XYL. In this plot, ρ_c was calculated taking only LTG:GaAs and n++ GaAs layers into consideration. (ρ_c of the overall nanocontact structure including XYL layer is discussed in later sections.)

Since the calculated ρ_c tends to decrease as the work function of Au cluster gets smaller and becomes close to the experimental value ($\sim 1 \times 10^{-6}$ $\Omega\cdot\text{cm}^2$) measured by STM, it is likely that the work function of Au nanocluster is smaller than that of bulk Au material. It has been reported that the work function of metallic material can be dependent on the size of clusters,[111,112] and this prior work suggests that the work function of nanoscale metallic cluster tends to increase as the size of isolated cluster decreases. However, it is possible that the work function may decrease in a different environment such as the case where a cluster is electronically coupled to a substrate because the single electron charging energy term in the work function decreases due to the larger capacitance that results when a cluster is coupled to a substrate. A few tenth of eV reduction in the work function of Au cluster significantly enhances the ohmic contact performance in the nanocontact structure. The argument based on the work function is at least consistent with

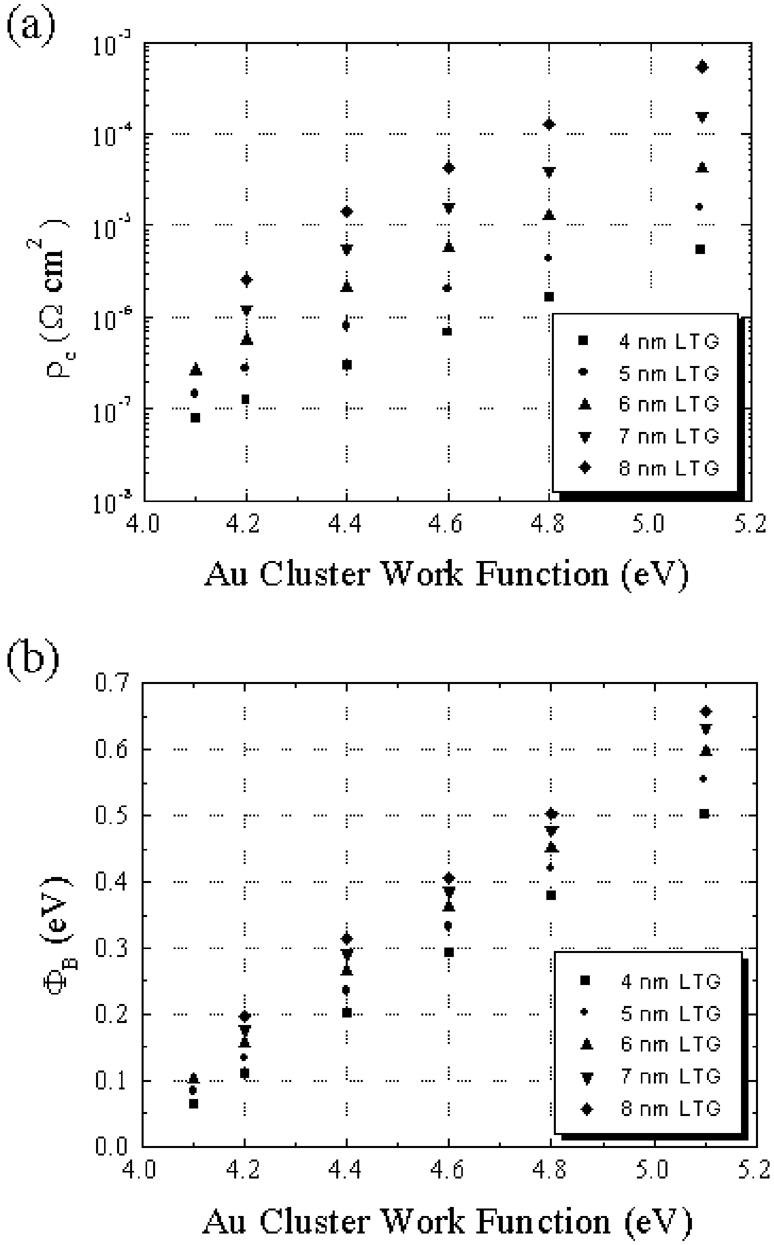


Figure 7.4

(a) Calculated specific contact resistance (ρ_c) and (b) barrier height (Φ_B) at LTG:GaAs interface versus the work function of Au nanocluster taking only LTG:GaAs (undoped) and n++ GaAs layers into consideration.

the observation that in most cases the measured I-V over as-grown LTG:GaAs or XYL-coated LTG:GaAs surfaces does not show ohmic behavior. In this case, the STM tip (Pt-Ir; 80 % Pt, 20 % Ir) acts as a metal contact. The higher work function of Pt ($\sim$ 5.8 eV) tends to cause higher barrier height, preventing ohmic contact behavior. However, without a reliable experimental data of work functions of Au clusters, this argument will remain as a question for further study. In this regards, the measurement of the work function of Au clusters as a function of the size of clusters is of particular interest, which can be studied using a technique such as Kelvin probe microscopy.[113]

7.4 Conduction Model for Ohmic Nanocontact

The performance of ohmic contact is determined by (i) barrier height at the semiconductor (LTG:GaAs) interface and (ii) barrier width ($\sim$ LTG:GaAs layer thickness). Fig. 7.5 shows plots of ρ_c as a function of barrier width (a) and barrier height (b) in a triangular barrier structure between two contacts, where the triangular barrier shown as inset can represent the conduction band profile of the undoped LTG:GaAs (See Appendix F for MATLAB program to calculate ρ_c). In these plots, ρ_c was calculated from standard current density versus voltage (J-V) relationship

$$J = \frac{2e}{h} \int_0^\infty dE \int \frac{dk_{||}}{(2\pi)^2} \left[f(-eV + E) - f(E) \right] T(E, k_{||}) \ , \tag{7.1}$$

which is widely used in mesoscopic physics.[31,114,115] In this equation, $E = E_z + E_{||}$, where z and $||$ are normal and parallel direction to the metal-semiconductor

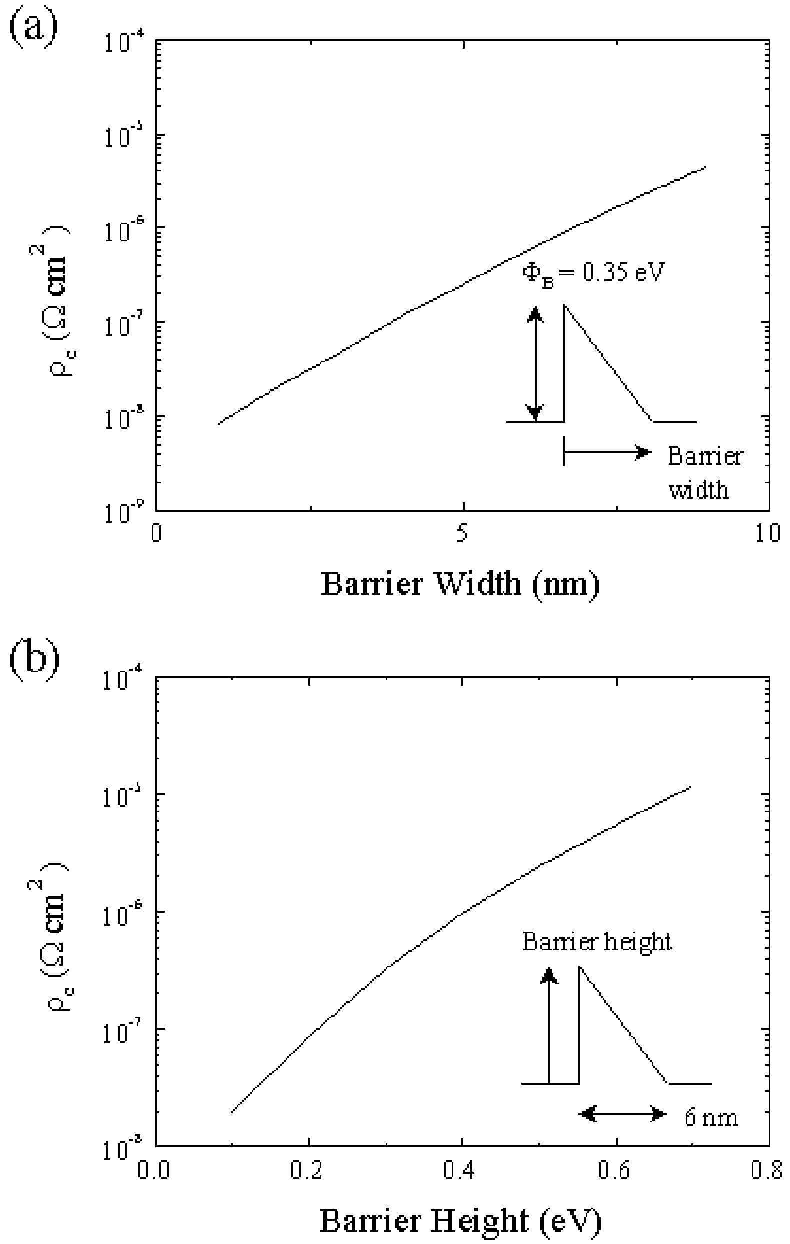


Figure 7.5

(a) Calculated ρ_c as a function of barrier width and (b) barrier height in a triangular barrier structure. The triangular barrier structure shown as inset, represents the conduction band profile of the undoped LTG:GaAs.

interface, respectively. f is the Fermi-Dirac distribution function and T is the transmission probability function. The integration ($\int dk_{||}$) can be converted into the integration over $E_{||}$ using 2-D density of states of metal contact as

$$\int \frac{dk_{||}}{(2\pi)^2}\,[f(-eV+E)-f(E)] = \frac{2\pi m}{h^2}\int_0^\infty dE_{||}\,[f(-eV+E_z+E_{||})-f(E_z+E_{||})] \ . \tag{7.2}$$

The integration can be evaluated analytically

$$\int \frac{dk_{||}}{(2\pi)^2}\,[f(-eV+E)-f(E)] = \frac{2\pi m k_B T}{h^2}\,\ln\left[\frac{1+\exp[(E_F-E_z+eV)/k_BT]}{1+\exp[(E_F-E_z)/k_BT]}\right] \ . \tag{7.3}$$

Therefore, J-V is simplified as

$$J = \int_0^\infty dE_z\,T(E_z)\,N(E_z) \ , \tag{7.4}$$

where $N(E_z)$ is given by

$$N(E_z) = \frac{4\pi m e k_B T}{h^3}\,\ln\left[\frac{1+\exp[(E_F-E_z+eV)/k_BT]}{1+\exp[(E_F-E_z)/k_BT]}\right] \ . \tag{7.5}$$

$T(E_z)$ can be obtained using WKB approximation as

$$T(E_z) = \exp\left[-2\int_0^{w(E_z)} dz\,\frac{\sqrt{2\,m^*\,(\Phi_\mathrm{B}(z)-E_z)}}{\hbar}\right] \ , \tag{7.6}$$

where $w(E_z)$ is barrier width at the turning point, $\Phi_\mathrm{B}(z)$ is barrier, and m^* is effective mass of electron within the barrier (LTG:GaAs).[87,116] By using $\Phi_\mathrm{B}(z)$ = Φ_B - (Φ_B/w_0) as the triangular barrier,

$$T(E_z) = \exp\left[-\frac{4w_0}{3\Phi_\mathrm{B}}\frac{\sqrt{2m^*}}{\hbar}(\Phi_\mathrm{B}-E_z)^{3/2}\right] \ , \tag{7.7}$$

where Φ_{B} is the barrier height at the metal-semiconductor interface and w_0 is the barrier width. By the definition, ρ_c is defined as

$$\rho_c^{-1} = [dJ/dV]\,|_{V\to 0} \ . \tag{7.8}$$

Therefore, the resulting expression for ρ_c^{-1} is

$$\rho_c^{-1} = \frac{4\pi m e^2}{h^3}\int_0^\infty dE_z\, T(E_z)\,\frac{1}{1+\exp[(E_z-E_F)/k_BT]} \ , \tag{7.9}$$

where $T(E_z)$ is given as Eq. (7.7).

WKB approximation breaks down when E_z is close to the barrier top ($E_z \simeq \Phi_{\mathrm{B}}$),[117] however WKB approximation is valid here because energies close to Φ_{B} can not contribute in the integral due to the Fermi-Dirac distribution function $1/\{1+\exp[(E_z-E_F)/k_BT]\}$. Only energies close to E_F can contribute.

Calculated ρ_c is plotted as a function of w with fixed $\Phi_{\mathrm{B0}} = 0.4$ eV (a) and as a function of Φ_{B0} with fixed $w = 6$ nm (b) in Fig. 7.5. Since the triangular barrier structure resembles the conduction band profile of LTG:GaAs layer in the nanocontact structure [see Fig. 7.3 (a)], the plots of Fig. 7.5 give information on the range of barrier widths and barrier heights in the nanocontact structure. To match the experimental ρ_c value ($\sim 1\times 10^{-6}$ $\Omega\cdot\mathrm{cm}^2$), the barrier width should be less than $\sim$ 6 nm as determined from Fig. 7.5 (a). This implies that LTG:GaAs layer should be reduced below the assumed 8 nm thickness to match the calculated ρ_c with the experimental value. The argument of further reduction in the barrier width (LTG:GaAs layer) is supported by considering conduction assisted by the midgap band of defects states (midgap states) as if it effectively reduces the barrier width. In the large area contact, midgap states do not play an important role in the ohmic contact. The large area ohmic contact structure with thin (< 5 nm) LTG:GaAs layer was mainly due to the direct tunneling from metal into GaAs layers.[108] However, when the LTG:GaAs layer increases, midgap states get more involved in the overall conduction. If the midgap states reduce the barrier width effectively by a few nanometers, the calculated ρ_c matches the experimental results. For example, when 6 nm thick LTG:GaAs layer was used for the calculation (with 4.6 eV as the work function of Au cluster), ρ_c of $\sim 1 \times 10^{-6}$ $\Omega\cdot\mathrm{cm}^2$ was determined from Fig. 7.5 (a).

In the next section, the effect of XYL layer in the nanocontact structure is discussed.

7.5 Effect of XYL in Ohmic Nanocontact

As concluded in the previous section, the mechanism in the ohmic nanocontact is mainly the direct tunneling from Au cluster into GaAs layers while the conduction is assisted by midgap states in LTG:GaAs layer. However, XYL layer was not considered for the ρ_c calculation presented in Fig. 7.4 (a). Qualitatively, the XYL layer can be described as a leaky dielectric or “insulator” in a M-I-S structure (Au cluster/XYL/LTG:GaAs).

To examine the effect of XYL layer in the ohmic nanocontact structure, the XYL layer might be treated as a rectangular barrier for ρ_c calculation as shown in Fig. 7.6. In this figure, ρ_c is plotted as a function of barrier width of a triangular barrier (a) and effective mass of electron in a rectangular barrier (b) for a combined barrier structure of the rectangular and triangular barriers, where the rectangular and triangular barrier represent the XYL layer and the LTG:GaAs layer, respectively. For these plots, ρ_c was calculated by Eq. (7.9) in the previous section using the transmission function for the combined rectangular and triangular barriers as

$$T(E_z) = \exp\left[-\frac{2w_1}{\hbar}\sqrt{2m_1^*(\Phi_{\mathrm{B}1} - E_z)/\hbar^2} - \frac{4w_2}{3\Phi_{\mathrm{B}2}}\frac{\sqrt{2m_2^*}}{\hbar}(\Phi_{\mathrm{B}2} - E_z)^{3/2}\right] \quad , \quad (7.10)$$

where $w_1 = 0.9$ nm is barrier width, $\Phi_{\mathrm{B}1} = 2$ eV is barrier height, and m_1^* is effective mass of electron in the rectangular barrier (XYL), and w_2, $\Phi_{\mathrm{B}2} = 0.35$ eV, and $m_2^* = 0.07\ m_o$ (m_o: free electron mass) are the corresponding quantities in the triangular barrier (LTG:GaAs).

Calculated ρ_c is plotted in Fig. 7.6 as a function of w_2 with $m_1^* = m_o$ (a) and as a function of m_1^* with $w_2 = 6$ nm (b). In these plots, the calculated ρ_c does not match the experimental ρ_c using any value of w_2 and m_1^*. Therefore, this implies that the combined barrier structure does not represent the nanocontact structure. Since the triangular barrier represents the LTG:GaAs layer well as explained in the previous section, it can be concluded that the rectangular barrier does not represent the XYL.

This argument can be examined by studying the electronic properties of XYL between metal contacts (Au) using a simulation program, MolecularIV.[118] MolecularIV simulation provides, for example, density of states (DOS), transmission probability, and resistance of a molecule as a function of energy (See Appendix E

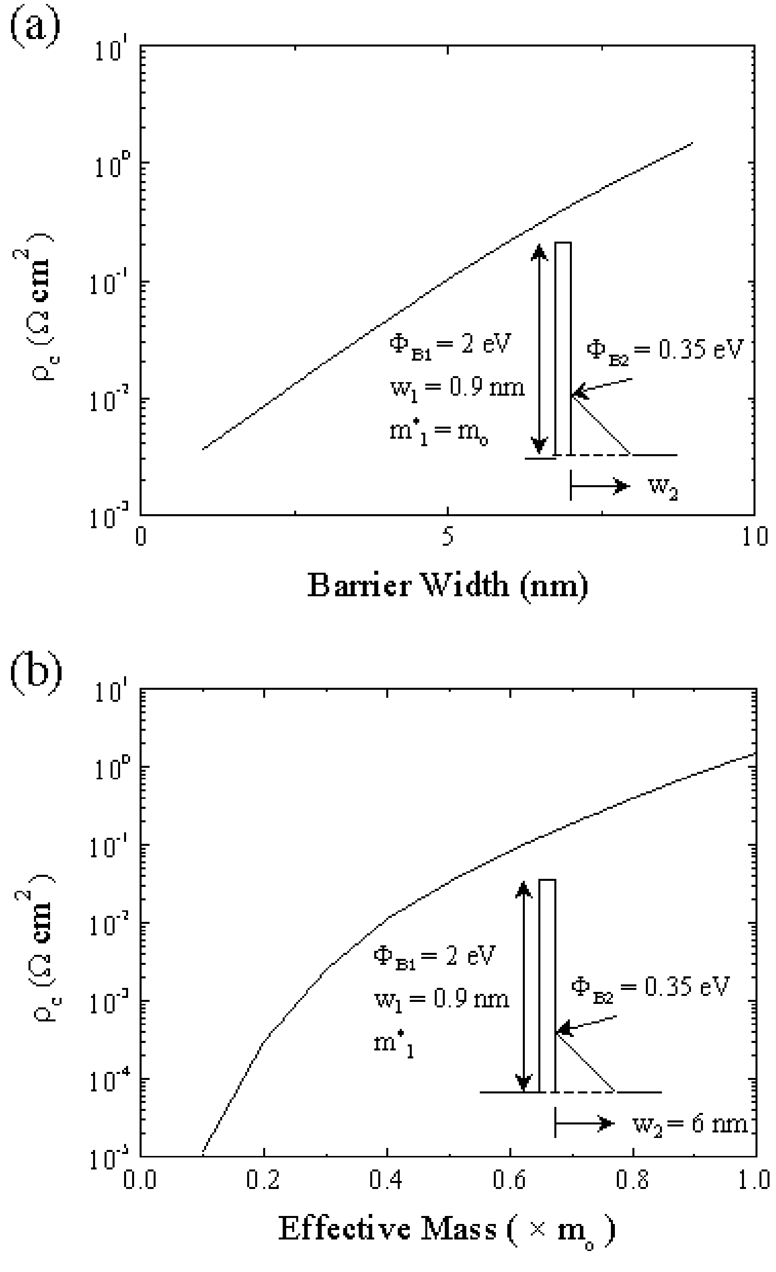


Figure 7.6

(a) Calculated ρ_c as a function of barrier width of a triangular barrier and (b) effective mass of electron in a rectangular barrier for a combined barrier structure of the rectangular and triangular barriers. The rectangular and triangular barrier represent the XYL layer and LTG:GaAs layer, respectively.

for MolecularIV simulation input file for XYL molecule). The rectangular barrier used for ρ_c calculation in Fig. 7.6 does not contain any finite density of states (DOS) within the bandgap, however XYL has finite DOS within the energy gap (HOMO-LUMO gap) as shown in Fig. 7.7 (a). Therefore, transmission probability of XYL within the energy bandgap is expected to be significantly larger than that of the rectangular barrier case. From Fig. 7.7 (b), the transmission probability around the Fermi level (E_F) is ~ 0.006. The transmission probability through the rectangular barrier can be calculated from the expression: $T = \exp\left[-2w_1\sqrt{2\,m_1^*\,\Phi_{\rm B1}}/\hbar\right]$. Using $w_1 = 0.9$ nm, $m_1^* = m_o$, and $\Phi_{\rm B1} = 2$ eV, T is found to be $\sim 2 \times 10^{-6}$ which is a few thousands times smaller than that of XYL at E_F. These properties of XYL (finite DOS in the energy gap and significantly larger transmission probability) indicate that XYL should not be treated as a rectangular barrier with zero DOS within the bandgap.

Furthermore, XYL layer is not quite insulating layer in the M-I-S nanocontact structure. From Fig. 7.8 (b), the resistance of XYL around E_F between Au contacts is ~ 2 MΩ. (~ 10 MΩ has been reported from experiments as the resistance of XYL-type of molecules.[5,119]) An equivalent contact resistance of XYL can be calculated with the resistance ~ 2 MΩ and the area per XYL molecule which is $\sim 2.5 \times 10^{-15}$cm^2 ($= 0.5$ nm $\times$ 0.5 nm). The equivalent contact resistance of XYL is found to be $\sim 5 \times 10^{-9}$ $\Omega{\cdot}$cm^2. This equivalent contact resistance of XYL is hundreds to thousands times better than the typical ohmic contact resistance on semiconductors ($\sim 10^{-6}$ $\Omega{\cdot}$cm^2).

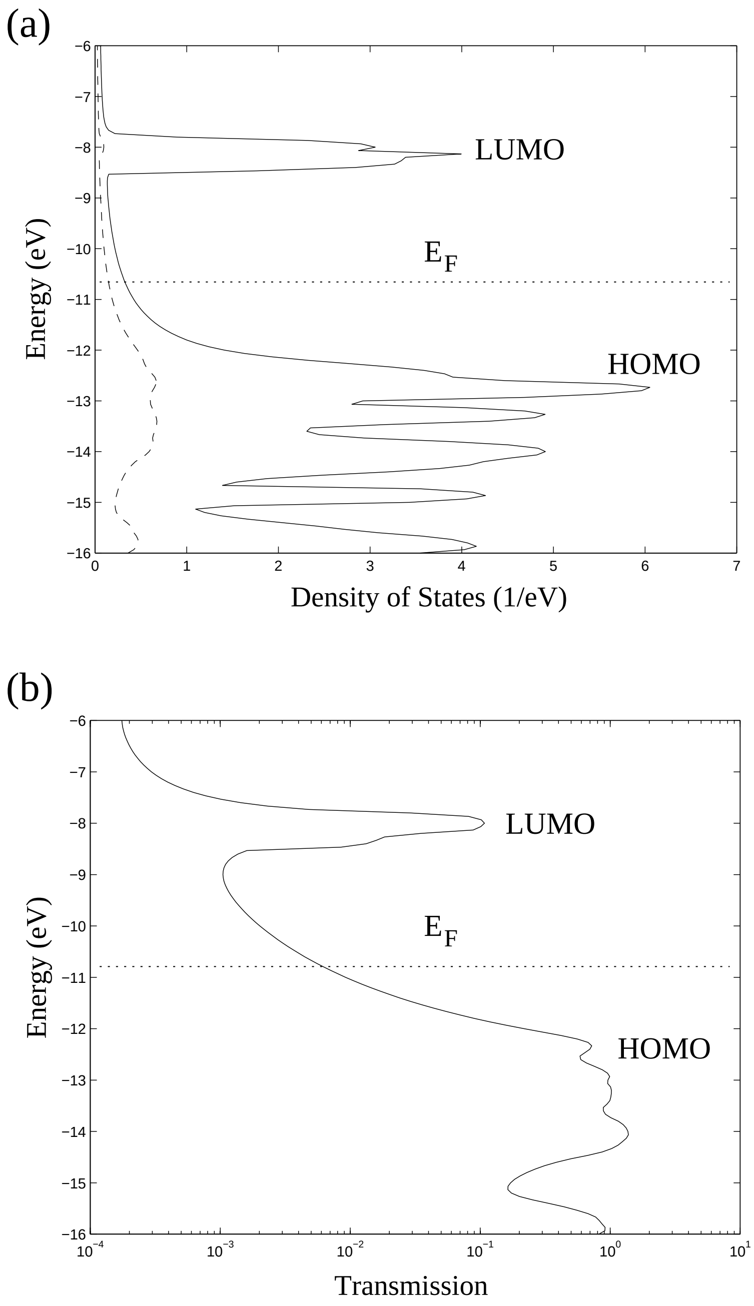


Figure 7.7

(a) Calculated density of states (as solid curve) and (b) transmission probability as function of energy for a XYL molecule between Au contacts. See Fig. 7.8 for the Fermi level (E_F) position of XYL.

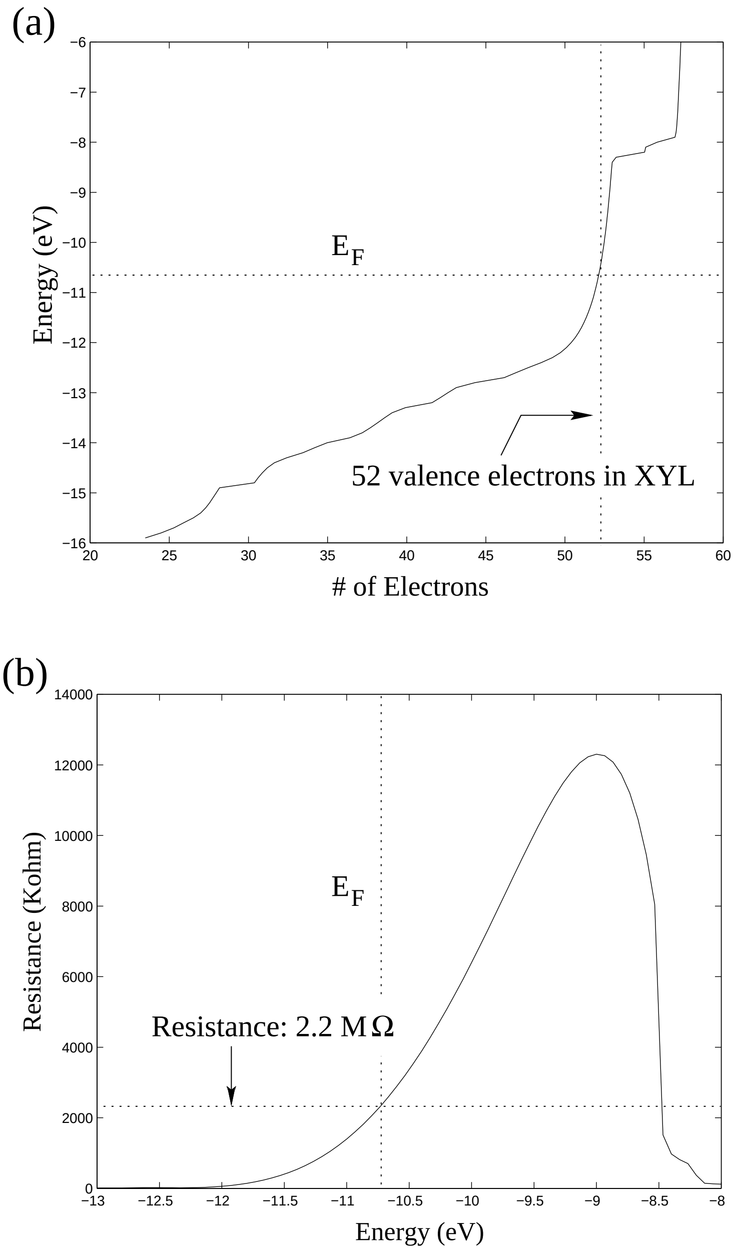


Figure 7.8

(a) Calculated number of electrons and (b) resistance as a function of energy for a XYL molecule between Au contacts. E_F is determined by the total number of valence electrons in XYL which is 52 electrons (S-CH_2-C_6H_4-CH_2-S without hydrogen atoms at each end of XYL due to S-Au bonding). Resistance of XYL at E_F is $\sim$ 2.2 MΩ.

Therefore, XYL layer should not be treated as an insulating layer in the M-I-S nanocontact structure. Instead, it is a quite conductive layer which mechanically tether Au nanocluster onto the ohmic contact structured LTG:GaAs layer surface. In this regards, the calculated ρ_c in Fig. 7.4 (a) can approximate the actual ρ_c of the nanocontact structure including XYL layer.

As a rough estimation, the transmission probability of XYL between Au contacts (Fig. 7.7) can be used in Eq. (7.10) to predict ρ_c of the nanocontact structure. The new $T(E_z)$ is

$$T(E_z) = T_1(E_z) \times T_2(E_z) \simeq 0.006 \times \text{Eq. (7.7)} \ , \tag{7.11}$$

where $T_1(E_z)$ and $T_2(E_z)$ are the transmission probability for the XYL and LTG:GaAs, respective. 0.006 is the transmission probability of XYL between Au contacts around E_F. A constant transmission probability 0.006 can be used as $T_1(E_z)$ since only energies close to E_F can contributes in the ρ_c calculation due to the Fermi-Dirac function in Eq. (7.9) and the transmission probability of XYL does not change significantly as energies around E_F [see Fig. 7.7 (b)]. For a more realistic ρ_c, XYL needs to be treated quantitatively, for example by incorporating the energy-dependent transmission probability of XYL between Au and GaAs layer, which remains as a further study.

The calculated ρ_c is plotted in Fig. 7.9 (a) as a function of the barrier width of the triangular barrier (LTG:GaAs) using $\Phi_{\mathrm{B2}} = 0.35$ eV. When 6 nm thick LTG:GaAs is used as the barrier width, the calculated ρ_c is $\sim 8 \times 10^{-5}$ $\Omega\cdot\text{cm}^2$

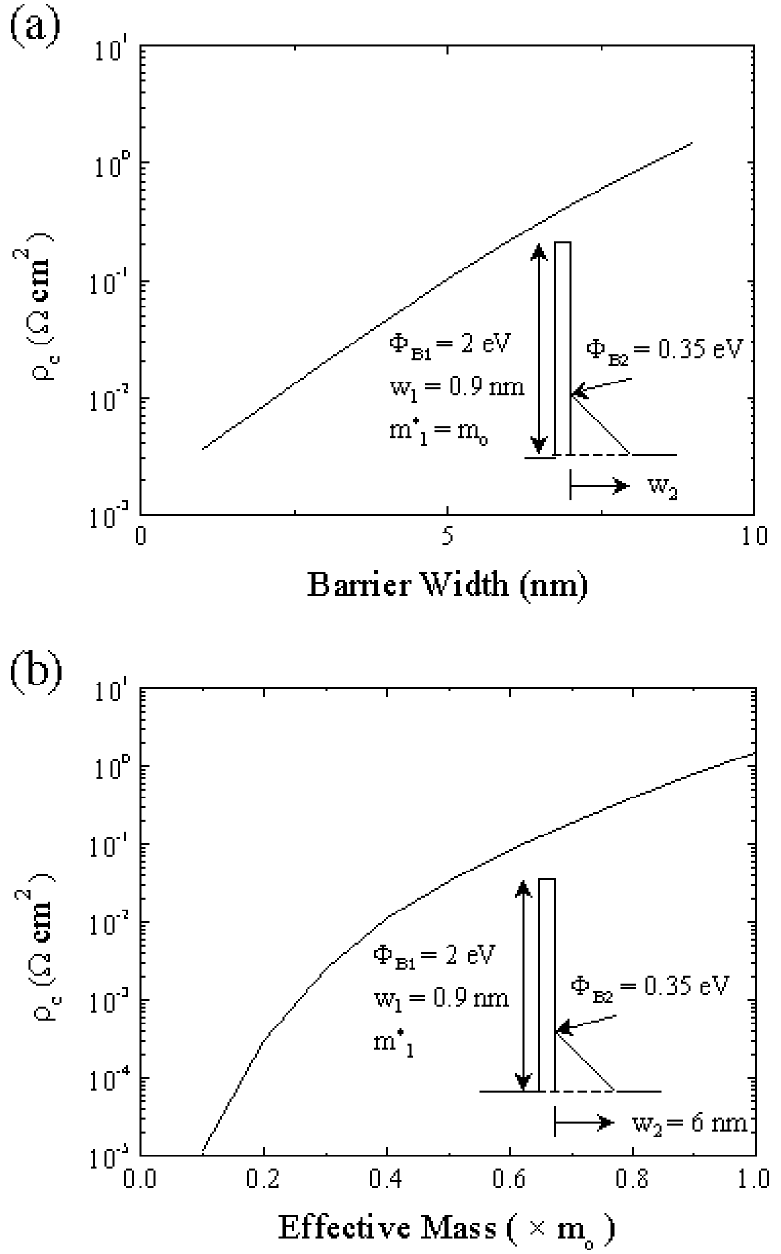


Figure 7.9

Calculated ρ_c as a function of barrier width of a triangular barrier. The transmission probability (0.006) of XYL at E_F between Au contacts was used in this calculation by Eq. (7.11) with Φ_{B2} = 0.35 eV (a) and 0.25 eV (b).

which is almost two order of magnitude higher than the measured ρ_c from the nanocontact structure.

In Fig. 7.9 (b), ρ_c is calculated using $\Phi_{\mathrm{B2}} = 0.25$ eV. When the barrier width is less than 5 nm, the calculated ρ_c is within the same order of magnitude of the experimental ρ_c. However this kind of barrier structure as LTG:GaAs is not realistic because Φ_{B2} of 0.25 eV is too low.

In next section, a new conduction mechanism is considered as the proper conduction mechanism for the nanocontact structure.

7.6 Sequential Tunneling Mechanism

In the previous section, a direct tunneling through the XYL and LTG:GaAs layer as one tunneling barrier was used as the main mechanism in the conduction model for the nanocontact structure. This is different from a case when the XYL and LTG:GaAs layer act as two resistors connected in series. In this case, the conduction mechanism is a sequential tunneling through each barrier.

The sequential tunneling is believed to be the proper conduction mechanism on the nanocontact structure by considering the density of states (DOS) at the XYL-LTG:GaAs interface, which is schematically illustrated in Fig. 7.10. The DOS for the midgap states in the XYL-LTG:GaAs interface and the DOS in the n++ GaAs layer within a few $k_B T$ around the Fermi level are calculated to be $\sim 5 \times 10^{18}$ cm^{-3} and $\sim 1 \times 10^{18}$ cm^{-3}, respectively, which are comparable to each other.[108] Therefore, electrons coming from Au contact into the LTG:GaAs

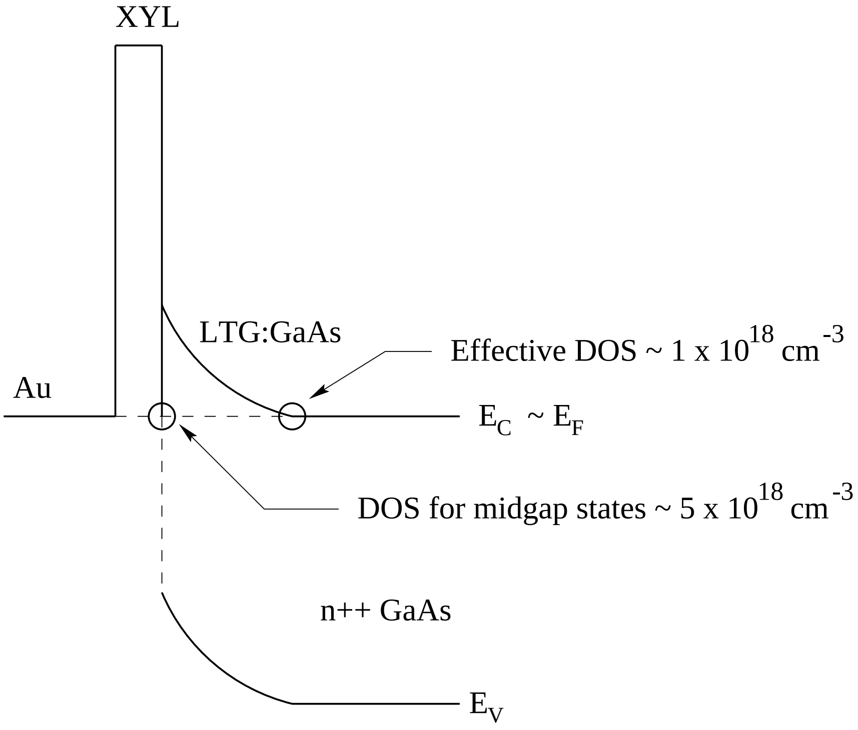


Figure 7.10

Energy band diagram illustrating the density of states (DOS) at the XYL-LTG:GaAs interface and the n++ GaAs layer within a few k_BT around the Fermi level (E_F).

layer tunnel through the XYL barrier and stay in the midgap states at the XYL-LTG:GaAs interface, and then tunnel through the LTG:GaAs barrier into n++ GaAs layer. This results in the sequential tunneling conduction.

For the sequential tunneling, the conductance G for the nanocontact is $(G_1 \times G_2)/(G_1 + G_2)$ where G_1 is the conductance of the XYL and G_2 is the conductance of the LTG:GaAs. Current density vs voltage (J-V) can be calculated for each case using Eq. (7.4): J_1-V_1 for the XYL barrier ($T_1 = 0.006$) and J_2-V_2 for the LTG:GaAs barrier [T_2 = Eq. (7.7)], as shown in Fig. 7.11 (See Appendix F for MATLAB program to calculate J-V). In the sequential tunneling, $J = J_1 = J_2$ and $V = V_1 + V_2$. J-V can be obtained from V-J by adding V_1 and V_2 as a function of J. In order to find V_1-J and V_2-J, first J is selected from J_2, then V_1 can be found as a function of J by using a linear interpolation. For example, when a J_2 value is between two J_{1a} and J_{1b} values ($J_{1a} < J_{1b}$), V_1 at J_2 is

$$V_1 \text{ at } J_2 = (J_2 - J_{1a})/(J_{1b} - J_{1a}) \times (V_{1b} - V_{1a}) + V_{1a} \quad . \tag{7.12}$$

Fig. 7.12 shows the calculated J-V (solid) for the nanocontact structure in this way. For the comparison, the measured J-V was included (+ marked) in the plot. The measured J-V curve was obtained by assuming the contact area (the area of cluster facet) of 6.3×10^{-14} cm^2. (The facet area of 4 nm diameter truncated octahedral Au cluster is $\sim 9 \times 10^{-14}$ cm^2.) The voltage value of the measured J-V must represent the actual voltage amount dropped across only the nanocontact structure, not the voltage amount applied between STM tip and sample. The

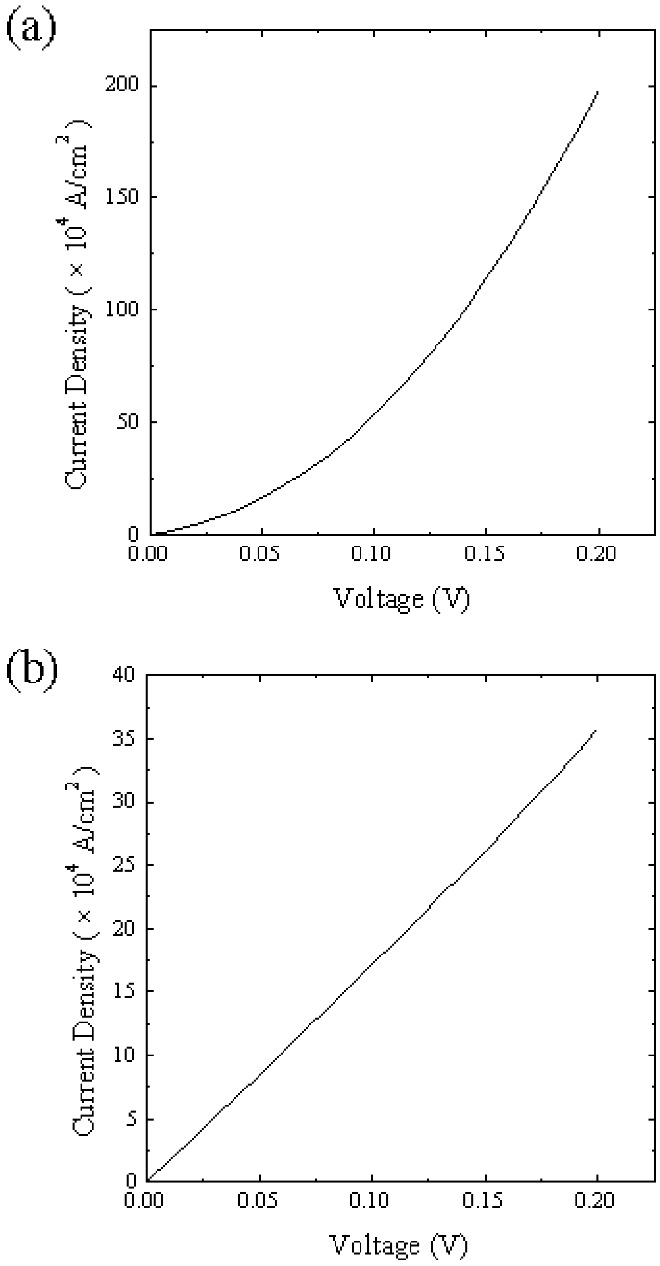


Figure 7.11

Calculated J_1-V_1 for the XYL barrier (a) and J_2-V_2 for the XYL barrier (b).

actual voltage amount dropped across the nanocontact can be calculated using the voltage division factor ($\sim$ 0.21) described in chapter 6. As shown in this figure, the calculated and measured J-V curves are in a good agreement, indicating the sequential tunneling mechanism is the right conduction model. In this curve, the voltage is the applied sample bias, therefore the J-V represent the characteristic in the reverse-bias region in M-I-S contact structure. The calculation of J-V in the forward-bias region requires both tunneling (field emission) and thermionic emission, which remains as a further study.

From the J-V curve in Fig. 7.12, the specific contact resistance can be calculated by the slope of a linear fit. (The calculated J-V curve is fitted with a straight line of $J = A + B \times V$: A = -10102, B = 1219751.) From the inverse of the slope of the straight line, the specific contact resistance was found to be $\sim 8 \times 10^{-7}$ $\Omega\cdot$cm^2 which is also in a good agreement with the experimental ρ_c having an upper bound of $\sim 1 \times 10^{-6}$ $\Omega\cdot$cm^2 and a lower bound of $\sim 7 \times 10^{-7}$ $\Omega\cdot$cm^2 (see Table 6.2).

Therefore, the sequential conduction mechanism explains both J-V and specific contact resistance measured on the nanocontact structure from STM experiments.

7.7 Nanocontacts on Undoped LTG:GaAs vs Be-doped LTG:GaAs

The last question in the ohmic nanocontact structure is why the nanocontact on Be-doped LTG:GaAs has higher ohmic contact properties compared to those in the nanocontact on the undoped LTG:GaAs. I-V measurements (Fig. 6.11) and

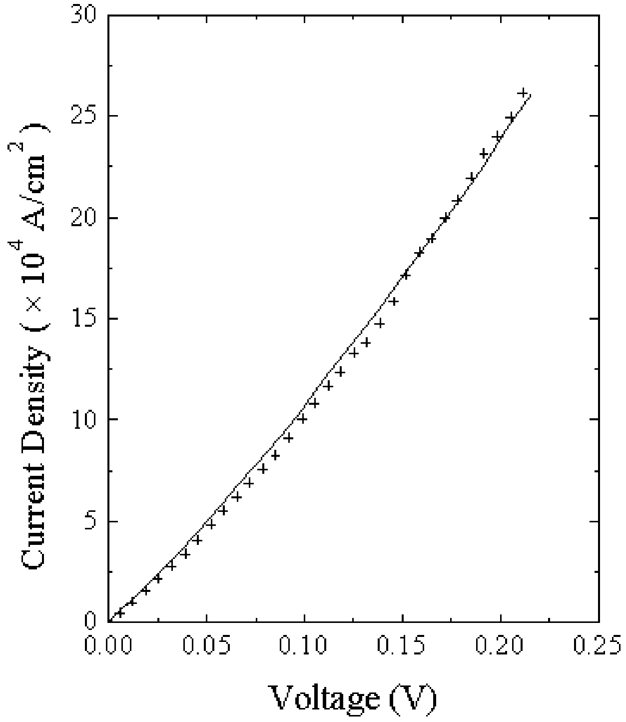


Figure 7.12

Calculated J-V (solid) and measured J-V (+ marked) for the nanocontact structure.

I-z measurements (Fig. 6.14) indicated that nanocontacts on Be-doped LTG:GaAs had superior ohmic contact performance (see also Table 6.2).

This superior ohmic contact performance for the nanocontacts on Be-doped LTG:GaAs can be understood by (i) surface chemical stability and (ii) midgap states of Be-doped LTG:GaAs. Several observations of the relative stabilities of organic monolayers on undoped and Be-doped layers of LTG:GaAs indicate that the Be-doped layers are chemically more stable and therefore the nanocontact samples with Be-doping in the LTG:GaAs surface layer may have a lower interface state density than those in the samples with undoped surface layer.[79] Ellipsometry measurements also indicate an improved stability of Be-doped over undoped LTG:GaAs.[79]

For example, Holden, et al.[120] studied the surface band bending of thick Si-doped (as n-type dopant) and Be-doped (as p-type dopant) LTG:GaAs surface layers without XYL (Si-doped LTG:GaAs is similar to undoped LTG:GaAs). Following prolonged air exposure, the Si-doped LTG:GaAs layer showed midgap (0.7 eV) surface Fermi level pinning. The band bending in Be-doped LTG:GaAs is still n-type (upward band bending) as a consequence of the large number of donor-like defects, but it was nearly flat, indicating a reduced surface-state (charge) density in the Be-doped LTG:GaAs. This implies an improved surface stability, i.e. less oxidation and fewer surface states, for the Be-doped LTG:GaAs.

However, unlike an early study,[79] the reduced surface state density in Be-doped LTG:GaAs may not correspond to a lower barrier height for electron tunneling.

Since the Fermi level is located $\sim$ 0.7 eV below the conduction band edge in Be-doped bulk LTG:GaAs material (see Fig. 7.1), the surface barrier height at Be-doped LTG:GaAs will be also $\sim$ 0.7 eV, which is larger than that at unpinned undoped LTG:GaAs ($\sim$ 0.3 eV). Similarly, in the nanocontact structures the surface barrier height at Be-doped LTG:GaAs was also determined to be larger than that at undoped LTG:GaAs (see Fig. 7.3). Therefore, the surface barrier height does not play an important role against the ohmic contact.

Contrary to the surface barrier height, midgap states in LTG:GaAs layer can explain the difference in the ohmic contacts between two samples. A significantly large amount of the midgap states are distributed around the Fermi level in the nanocontact on Be-doped LTG:GaAs which result in midgap states-assisted conduction [Fig. 7.3 (b)], while the midgap states are located relatively below the Fermi level in the nanocontact on undoped LTG:GaAs [Fig. 7.3 (a)]. When Au cluster contact is made on Be-doped LTG:GaAs, current conduction is assisted by the midgap states distributed around the Fermi level and electrons will tunnel through the rest of barrier in Be-doped LTG:GaAs layer as if this layer is reduced more effectively than undoped LTG:GaAs layer due to the midgap states.

The midgap states-assisted conduction is consistent with a STM study by Feenstra, et al.[66] where they observed a peak of midgap states below the Fermi level in Si-doped LTG:GaAs and double peaks straddling the Fermi level in Be-doped LTG:GaAs. Any states around the Fermi level in Be-doped LTG:GaAs can contribute to conduction.

Therefore, midgap states play an important role in the superior ohmic contact behavior in the nanocontact structures on Be-doped LTG:GaAs while overall conduction is the sequential tunneling mechanism in both cases.

8. SELF-ASSEMBLED 2-D ARRAYS OF Au NANOCLUSTERS

8.1 Introduction

Individual Au nanocluster as ohmic contact on GaAs has a potential on nanoelectronic device contact structure on semiconductors. However, the demand of fabricating Au nanoclusters on semiconductor surfaces in an ordered 2-D structure is stringent for the realistic nanoscale device applications. It is widely recognized that self-assembly techniques offer the potential to fabricate nanoscale elements in an ordered structure without direct use of conventional lithographic techniques which become expensive and slow when used to define nanoscale features. A number of self-assembly techniques have been reported for fabricating nanometer scale structures of clusters, quantum dots, and wires.[18–26,121] Thus, nanoscale structures resulting from self-assembly techniques may potentially provide the basis of a non-lithographic approach for fabricating nanoelectronic devices and circuits. The types of structures reported to date, including uniform, large area arrays of clusters and structures such as cluster dimers and trimers,[122] provide interesting configurations, but are not sufficient to provide sophisticated electronic circuits. The realization of electronic circuits of reasonable functionality and complexity using self-assembly approaches will require the ability to controllably break the symmetry typically found in self-assembled networks or to assemble the building blocks (e.g. nanometer-size clusters) into specific configurations as well as the ability to realize devices with functionality comparable to current semiconductor devices. An interesting approach would be to combine the nanoscale elements and ordering from self-assembly processes with a procedure which can impose a somewhat arbitrary larger-scale pattern to form the specific configurations and interconnections needed for computation.

Toward this goal, high-quality close-packed arrays of Au nanoclusters (~ 5 nm in diameter) have been formed in patterned regions on active GaAs substrates employing LTG:GaAs cap layer and characterized using STM.[123] The approach utilizes a patterned template which guides the self-assembled elements into preselected regions with a molecular tether (XYL). The local ordering at the nanometer scale is provided by a chemically driven self-assembly process, while the arbitrary global pattern is defined by the patterned template with a soft lithographic technique. The directed self-assembly techniques used to fabricate these structures have the potential to provide high-throughput fabrication of structures for nanoelectronics and other nanoscale applications.

In this chapter, the directed self-assembly fabrication of patterned self-assembled array of Au nanoclusters is described and the characterization of the structural and electronic properties of the resulting network is discussed.

8.2 Unpatterned Self-Assembly of Au Nanocluster Arrays on GaAs

(The self-assembled Au nanocluster arrays was fabricated on GaAs by Jia Liu.[123,124])

A simple method to form arrays of Au nanoclusters is to case a few drops of a colloidal solution containing nanoclusters on a flat solid substrate. As the solvent evaporates, the nanoclusters spontaneously organize into arrays. There are many examples of Au nanoclusters arrays studied by STM that have been fabricated on a variety of different substrates, but in most cases, the arrays are not formed on semiconductors. For examples, Au nanocluster arrays have been fabricated on MoS_2[18] and on Au film.[125,126]

The drop casting method however cannot be used to fabricate large area, well-ordered arrays of nanoclusters. To form large area, well-ordered monolayer arrays of clusters, a new technique was developed, as illustrated in Fig. 8.1. Monolayer arrays are first formed on a water surface, then transferred from the water surface to a solid substrate. Gold citrate sols were purchased from British BioCell International (Part number: EM.GC5). The Au nanoclusters were then encapsulated with DDT. A concentrated hexane solution of DDT encapsulated Au nanoclusters with a tight size distribution was cast onto the water surface. Upon solvent evaporation, the Au nanoclusters spontaneously organize into a hexagonal close-packed monolayer array at the air/water interface due to the Van der Waals attraction between clusters.[127,128] This monolayer can be transferred onto a solid substrate by touching it with the substrate briefly.

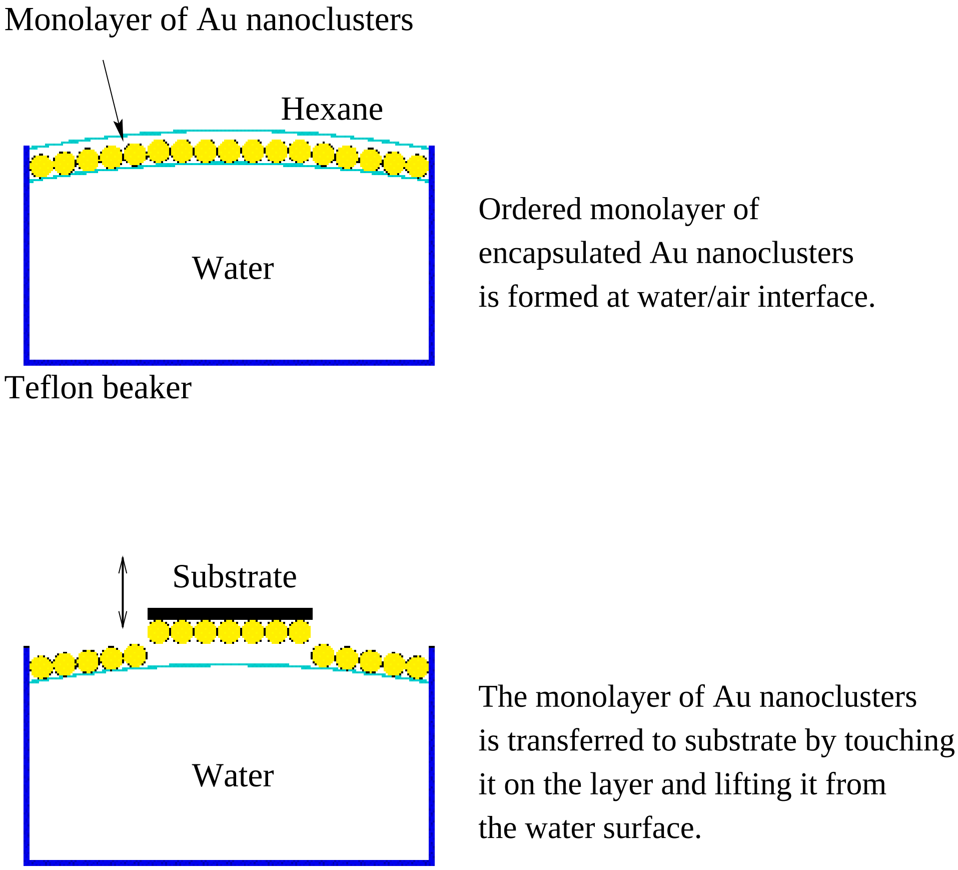


Figure 8.1

A schematic illustrating the process that a well-ordered monolayer array of DDT encapsulated Au nanoclusters is formed at water/air interface and is transferred to a solid substrate by touching it on the layer and lifting it from the water surface.

In order to verify the local and long-range ordering of the cluster arrays, the arrays were transferred to an amorphous carbon film supported on a copper grid. A typical TEM micrograph of such a monolayer array is shown in Fig. 8.2 and reveals a hexagonal close-packed array of Au nanoclusters. (TEM study was performed by Jia Liu.) The relative orientation of this array is preserved over microns, with a cluster vacancy density of $\sim 10^{-4}$ times the cluster density ($\sim 2 \times 10^{12}$ clusters/cm^2). The Au nanoclusters are found to have a mean diameter of 5.2 ± 0.6 nm and an average edge-to-edge spacing of 3.1 ± 0.2 nm. This spacing between neighboring clusters is close to twice the molecular length of DDT ($\sim$ 1.6 nm), indicating that DDT molecules surrounding each Au nanocluster are nearly fully extended. This process is significantly different from the previous observations that DDT molecules were interdigitated in arrays of Au or Ag nanoclusters formed directly on solid substrates,[18,129] and indicates a significant weakening of any cluster-cluster interactions in the lateral plane.

Even though highly ordered hexagonal close-packed arrays of Au nanoclusters can be transferred from water surface onto the amorphous carbon film supported on a copper grid for the TEM study, this type of substrate does not incorporate device functionality provided by semiconductor materials. Hence, comparable Au nanocluster monolayer arrays were transferred onto the ohmic contact structured LTG:GaAs substrate (10 nm thick) coated with XYL tether molecules. In order to allow the XYL molecules to chemically bond to the Au nanoclusters, the substrate was immersed in acetonitrile, a known non-solvent for the encapsulated

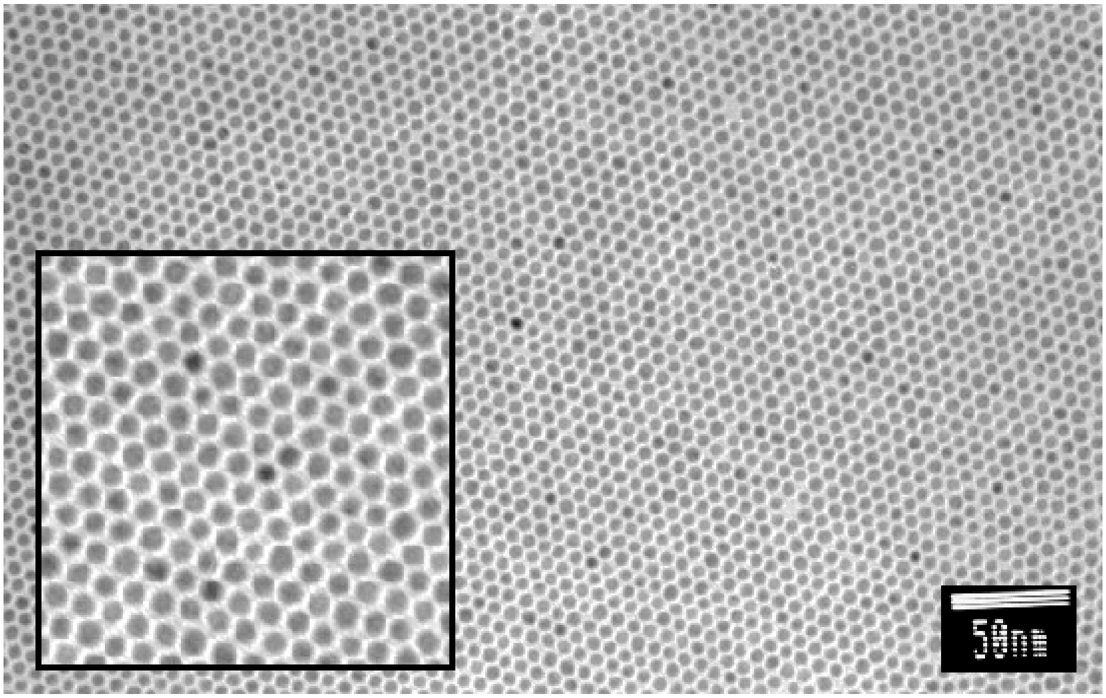


Figure 8.2

A TEM micrograph of a hexagonal close-packed monolayer array of DDT encapsulated Au clusters (5 nm in diameter) transferred from a water surface to a carbon TEM grid. The inset is a 100 nm × 100 nm enlarged view of the cluster array.

Au clusters, for 16 hours in a dry nitrogen glovebox (from Vacuum/Atmosphere Company, Model name: Nexus One). Then, STM was used to study to resolve the hexagonal close-packed arrays of Au nanoclusters on LTG:GaAs and probe the electronic properties of individual clusters within arrays. TEM can not be used for this type of substrate. Fig. 8.3 is a UHV STM image of Au nanocluster arrays transferred from water surface to a XYL-coated Be-doped LTG:GaAs substrate. A highly ordered hexagonal close-packed structure was observed. This image indicates that the interface layer of XYL provides a robust mechanical tethering of the Au nanoclusters to the LTG:GaAs surface and electronically links the Au clusters to the LTG:GaAs surface. Since the clusters were encapsulated by DDT, STM images were taken at low set currents (few hundred picoamps) and high sample bias voltages (approximately -1 V) to minimize the interaction between the STM tip and the DDT molecules. A center-to-center distance between neighboring clusters was determined to be 7.9 ± 0.6 nm by taking average among several STM images, consistent with the result obtained from the parallel TEM study ($\sim$ 8.3 nm) (see Fig. 8.2). The array extended over $\sim$ 0.1 μm, which is the maximum scan size of the UHV STM.

Representative *I*-*V* curves are shown in Fig. 8.4, for the case where the STM tip is over a cluster (solid curves marked A) and for the case where the STM tip is positioned between clusters (dashed curve marked B). As was observed in the experiment with isolated clusters for nanocontact structures, an ohmic behavior is observed when the tip is positioned over a cluster. As described in chapter 6, this

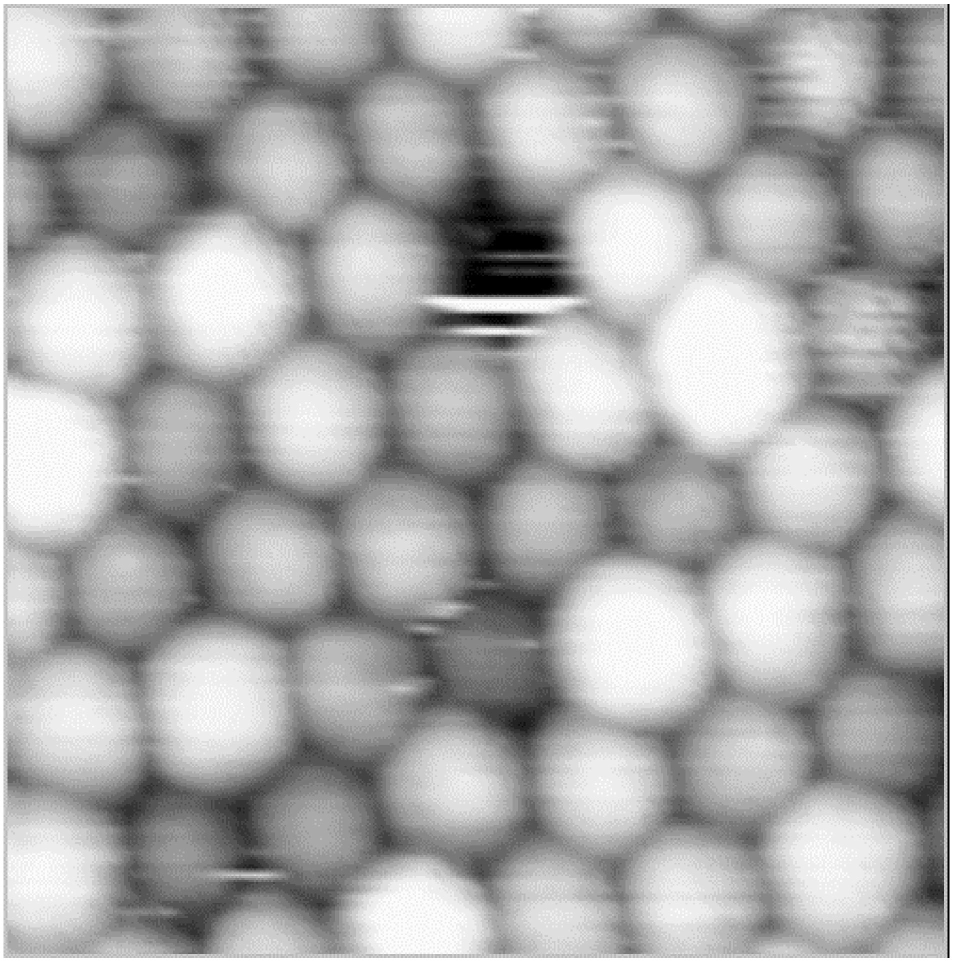


Figure 8.3

A 50 nm × 50 nm UHV STM topographic image of a hexagonal close-packed 2-D array of Au clusters tethered on the XYL-coated Be-doped LTG:GaAs, acquired with V_{set} = -1.2 V and I_{set} = 0.1 nA. There is a defect site (vacancy) in this image. Substrate is an ohmic contact structured Be-doped LTG:GaAs with 10 nm thickness.

ohmic behavior is because of the fact that most amount ($\sim$ 0.99 V) of the applied voltage (1 V) between tip and sample is dropped across tip-to-cluster interface due to the ohmic contact property on the cluster-to-semiconductor interface. The set-points, i.e. the V_{set} and I_{set} used to establish a relative tip height with respect to the local surface, is approximately the same in the "on cluster" and "off cluster" curves in order to allow reasonable comparison between the low-field current values. While the nature of the STM technique makes it difficult to ascribe absolute conductance values to the data, the fact that these trends persist to relatively high current level (when the tip is brought closer to the cluster) indicates that the conduction is enhanced when the current flows through a cluster. The I-V relationships for on-cluster sites within the array are comparable to those obtained on isolated clusters. The difference in shapes of the I-V curves between the case on and off a cluster is not as dramatic in the case of the cluster within the array as compared the case of isolated Au clusters (see Fig. 6.8 and 6.9). It is likely that there is some conductivity through adjacent clusters for the "off-cluster" curve in the array sample since the end size of the tip is 10-15 nm (see Fig. 4.7).

This observation is consistent with the fact that the cluster array used in this study is "unlinked", i.e. adjacent clusters within this array are separated by the DDT encapsulant and do not electrically communicate with each other. In this case, the coupling to the semiconductor substrate is much stronger than the inter-cluster (resistive) coupling. If adjacent clusters within the array were linked with a conductive molecule, it is expected that the intercluster resistance could be made

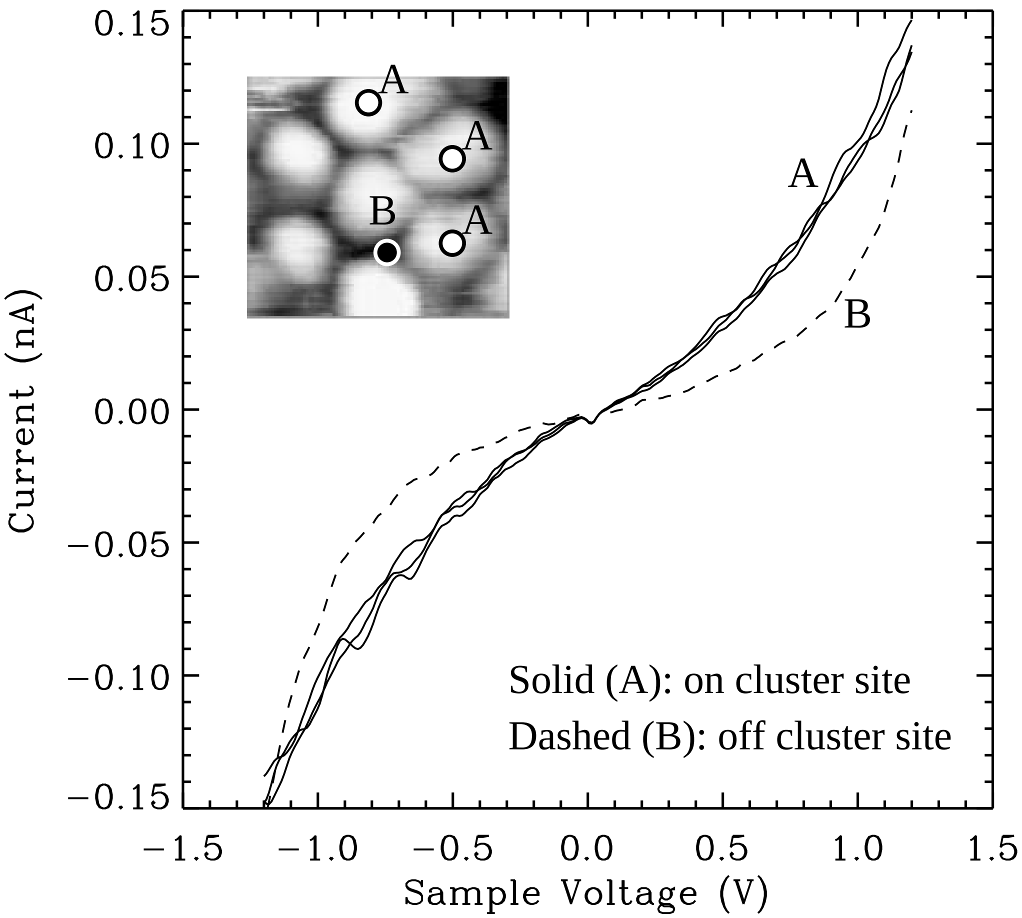


Figure 8.4

I-*V* data for Au clusters within an array tethered to a XYL-coated Be-doped LTG:GaAs surface (10 nm thick). Curves are taken with the STM tip positioned over three different clusters (A) and over an off-cluster site (B), acquired with I_{set} = 0.15 nA and V_{set} = -1.2 V. Locations of *I*-*V* scans are illustrated in inset, a 25 nm × 25 nm UHV STM image of the array acquired with I_{set} = 0.1 nA and V_{set} = -1.2 V.

comparable to the cluster-to-substrate resistance. In this case, I-V characteristics over the "on cluster" and "off cluster" sites will not be different. If the intercluster coupling is made much stronger than the cluster-to-semiconductor coupling, the resulting patterned array structure represents an interesting interconnect structure which has been described as a "molecular ribbon".[130]

For the ohmic contact on GaAs, relatively thin LTG:GaAs (< 10 nm) layer is required.[68,108] When a cluster array was transferred on a non-ohmic contact structured LTG:GaAs (100 nm thick), I-V on a cluster within the array is expected to show non-ohmic behavior. As expected, the STM I-V data over clusters within arrays on 100 nm thick LTG:GaAs sample showed a non-ohmic behavior with an energy bandgap, as shown in Fig. 8.5, which should be compared with the ohmic I-V over clusters within arrays on 10 nm thick LTG:GaAs sample (see Fig. 8.4). Since the LTG:GaAs layer is 100 nm thick, the cluster-semiconductor resistance is dominated by the bulk resistivity of this layer (approximately 10 $\Omega\cdot$cm).[131] A specific contact resistance of $\sim 1 \times 10^{-4}$ $\Omega\cdot\mathrm{cm}^2$ is estimated for this structure, and a substantial fraction (~ 0.5 V) of the applied voltage (1 V) between tip and sample is dropped across the cluster-semiconductor interface since the ratio R_2/R_{total} is around 0.5 ($R_{total} \simeq 1$ V/0.5 nA $= 2$ GΩ and $R_2 \simeq 1$ GΩ).

Therefore, non-ohmic behavior I-V measured on this sample reflects the energy bandgap of bulk LTG:GaAs material, and substantial changes in the conductance are expected versus bias for this case since the barrier between the cluster and the semiconductor is changed significantly.

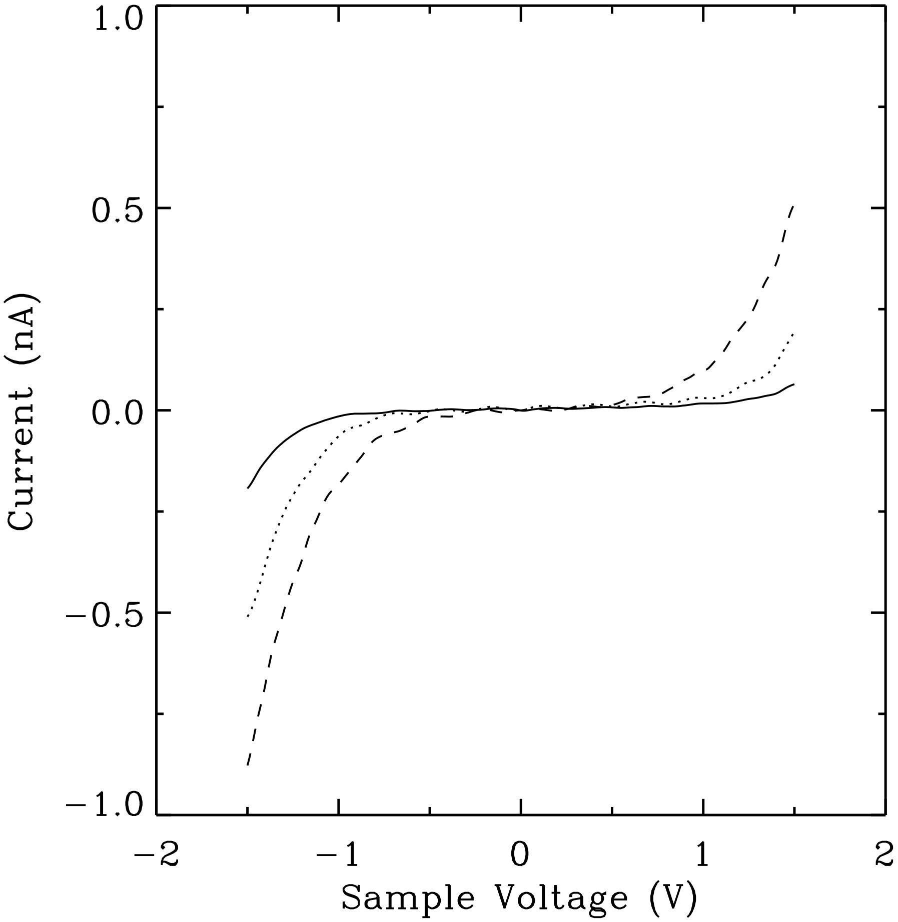


Figure 8.5

I-*V* data taken with STM tip positioned over on-cluster site within an array on non-ohmic contact structured GaAs layers (100 nm thick Be-doped LTG:GaAs cap layer), acquired with V_{set} = -1.5 V and I_{set} = 0.2 nA (solid), 0.5 nA (dotted), and 0.75 nA (dashed). All the *I*-*V* curves are not ohmic due to the substrate employing the non-ohmic contact structured GaAs layers.

8.3 Patterned Self-Assembly of Au Nanocluster Arrays on GaAs

Nanoelectronic device applications based on nanoclusters require a precise control in positioning of the nanoclusters onto semiconductor substrates. Several methods have been developed to realize this spatial positioning of nanoclusters. Vossmeyer, et al.[132] used light-directed, selective deposition technique to produce patterning of passivated Au nanoclusters (2.6 nm in diameter) on Si substrate. Electron-beam lithography or photolithography techniques was used to make prepatterned regions on SiO_2/Si substrate for deposition of passivated Au nanoclusters (2 nm in diameter).[133,134] Hung, et al.[135] used crystal strain and composition to direct assembly of nanoparticles (arsenic precipitates; 16 nm in diameter) within LTG:GaAs-based layers. They observed patterning effects of 1-D arrays of arsenic nanoparticles in LTG:GaAs layers. However, the studies reported to date have not realized well ordered structures such as close-packed arrays of nanoclusters and have not shown strong coupling between the nanoclusters and a semiconductor.

Toward this goal, (i) a guided self-assembly approach is utilized to realize structures of the type necessary for hybrid self-assembled/semiconductor circuits and (ii) high quality hexagonal close-packed monolayer arrays of Au nanoclusters are selectively deposited within patterned regions on a semiconductor surface (LTG:GaAs), with strong electronic coupling between the nanoclusters and the semiconductor substrate. In order to achieve well-ordered arrays at the nanoscale within regions of arbitrary patterns, a resistless lithography procedure is employed for predeposition of an organic tether molecule (XYL) on a chemically stable semiconductor surface layer (LTG:GaAs). The directed self-assembly fabrication technique used to form patterned cluster arrays involves (i) the deposition of an organic tether molecule in pre-defined regions on the semiconductor substrate, (ii) the transfer of a large area close-packed array of Au nanoclusters onto the substrate, and (iii) a solvent rinse to remove nanoclusters in regions not coated with the tether molecule. The resulting structure is schematically illustrated in Fig. 8.6.

The fabrication of patterned self-assembled Au nanocluster arrays on GaAs was performed by Jia Liu.[123,124] The GaAs substrate used for this study consisted of Be-doped epitaxial layers of stoichiometric GaAs, capped with a 100 nm thick layer of LTG:GaAs (see Fig. 8.6). A SAM of XYL was deposited in pre-defined regions on the LTG:GaAs substrate using the microcontact printing technique[136,137] as illustrated schematically in Fig. 8.7. A master plate consisting of an oxidized silicon wafer with the desired pattern was produced using photolithography and chemical etching of the oxide layer. To facilitate the release of stamp pad, the master plate was coated with a layer of octadecyltrichlorosilane (OTS) molecule by immersing in a dilute solution of OTS in anhydrous cyclohexane for an hour in dry nitrogen. Next, an 8:1(w:w) mixture of SYLGARD silicone elastomer 184 and SYLGARD silicone elastomer 184 curing agent (Dow Corning Corporation) was poured over the master plate and allowed to cure at room temperature overnight. The elastomeric polydimethylsiloxane (PDMS) stamp pad was then gently peeled off from the master plate. The working surface of the PDMS stamp pad contained the reverse image of the pattern that was formed in the master plate. The PDMS

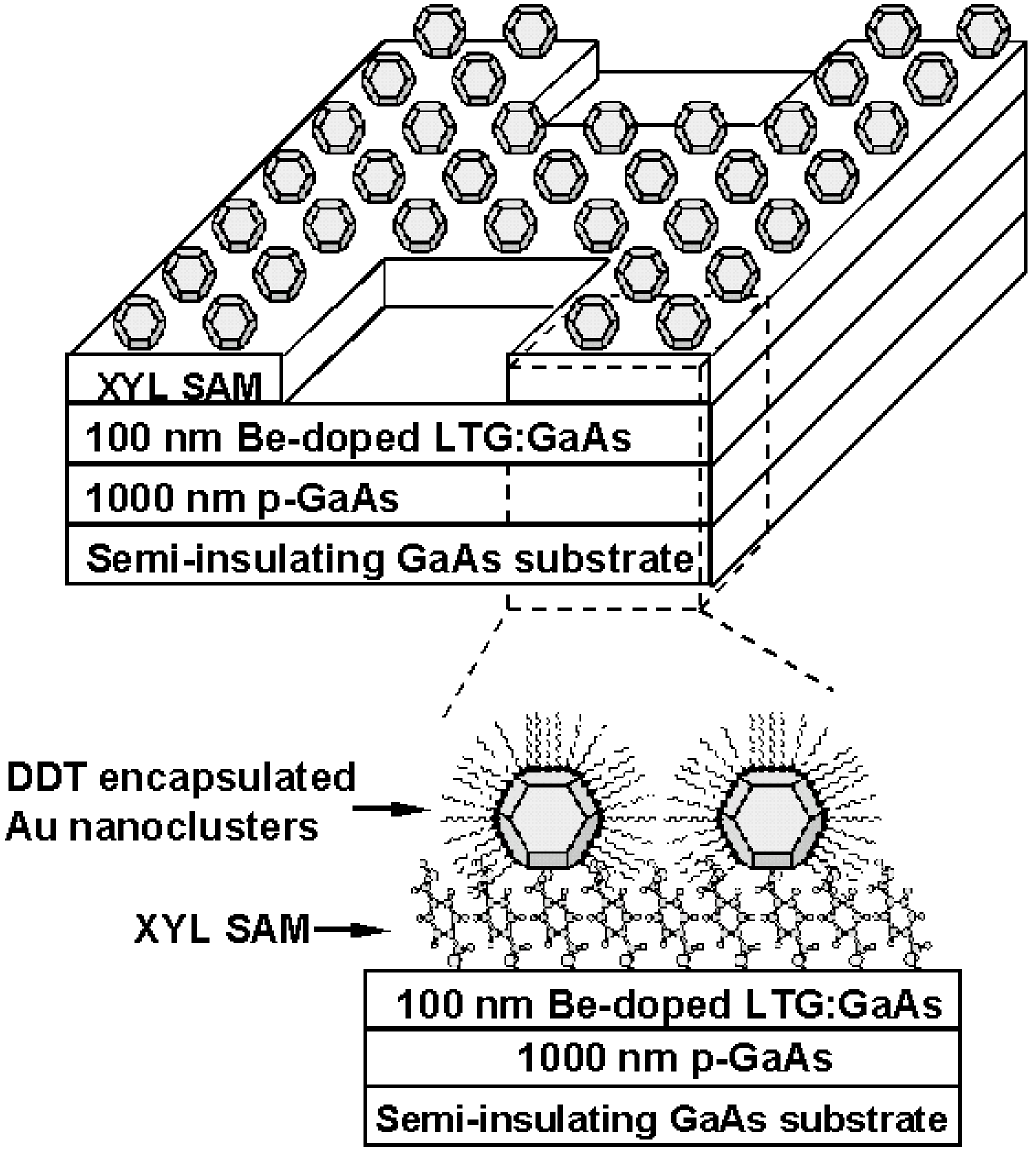


Figure 8.6

A schematic of close-packed array of Au nanoclusters formed in patterned regions on LTG:GaAs surface using a directed self-assembly fabrication technique. A 2-D array of DDT encapsulated Au nanoclusters is present only in regions coated with a tether molecule (XYL).

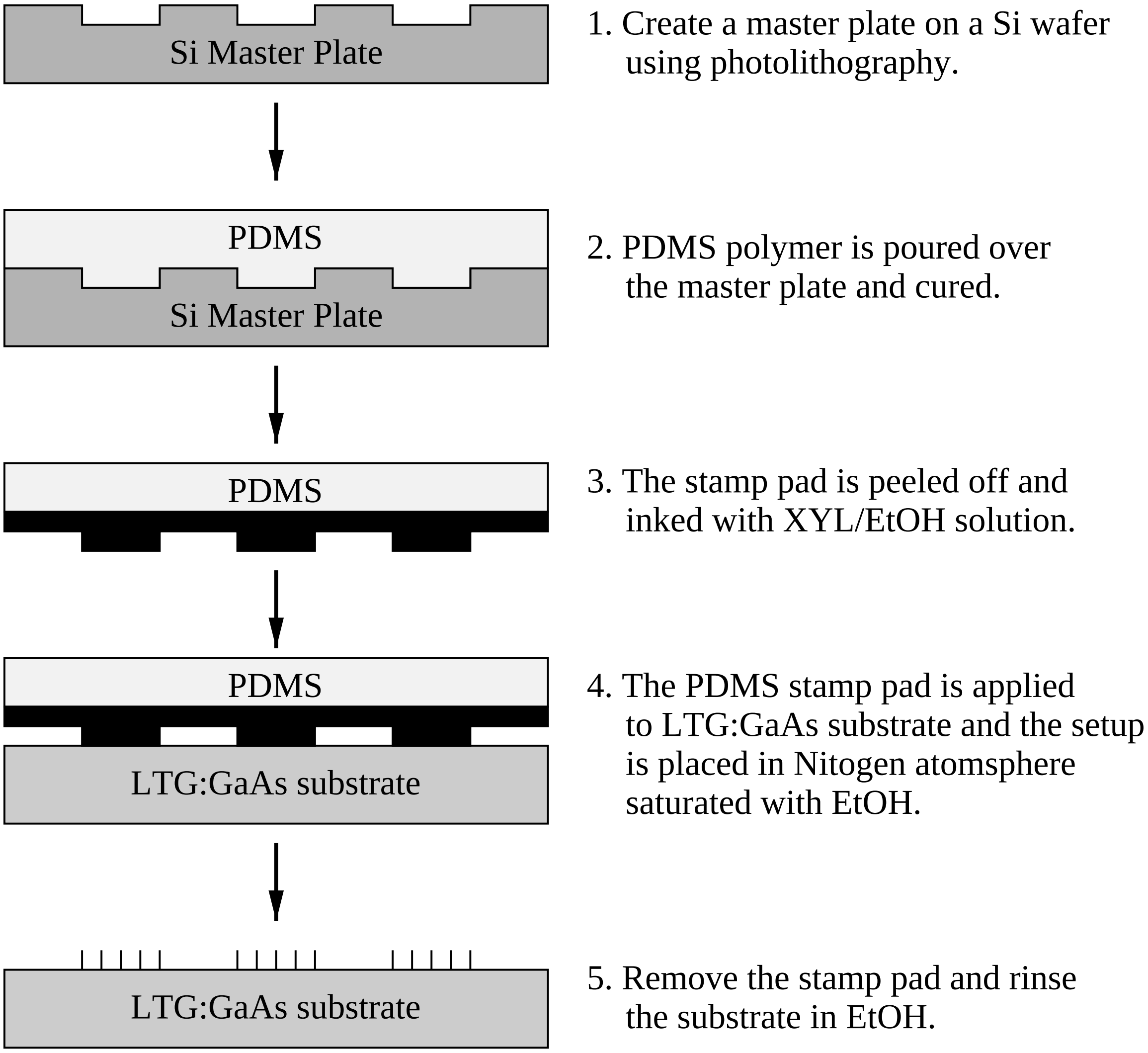


Figure 8.7

A schematic of patterning a SAM of XYL tether molecules on a LTG:GaAs substrate using the microcontact printing technique.

stamp pad was then immersed in a 1 mM solution of XYL in anhydrous ethanol for 5 minutes and removed. Any excess solvent on the surface of the elastomer was allowed to evaporate. The inked stamp pad was placed onto a LTG:GaAs substrate with the patterned surface facing the substrate. The setup was kept in a closed container saturated with ethanol vapor for 18 hours. Then the stamp pad was removed from the LTG:GaAs substrate and the substrate was thoroughly rinsed in ethanol. The above operations were all performed in a nitrogen atmosphere. The resulting structure consisted of an XYL SAM deposited only in those regions on the LTG:GaAs substrate where it touched the raised regions on the stamp pad. An ellipsometric image of patterned regions of XYL on LTG:GaAs using this microcontact printing technique was reported in an early study.[138] A scanning electron microscope (SEM) micrograph revealed a pattern etched into the LTG:GaAs protected by XYL layers using a wet etching.[138]

Previous studies have shown that SAMs of alkanethiols can be used as electron-beam photoresists on GaAs with resolutions below 10 nm.[139] In the current study a double-ended XYL SAM as a more chemically stable surface layer was used in order to provide a patterned tether. Conventional photoresist based techniques are generally not suitable for directing the self-assembly due to the associated nonplanarity of the surfaces, potential for molecular level contamination, and the possibility of interactions between the chemicals used in the photoresist processing and the self-assembly deposition.

The Au nanoclusters encapsulated with DDT dispersed in a nonpolar organic solvent (hexane) with a tight size distribution was cast onto a water surface to form a monolayer clusters arrays as described in the previous section. Au nanocluster monolayer arrays were then transferred onto the LTG:GaAs substrate which was previously patterned with XYL. The substrate was immersed in acetonitrile, a known non-solvent for the encapsulated Au clusters, for 16 hours in a high quality dry nitrogen glovebox. Then, the sample was rinsed in hexane, a good solvent for encapsulated Au clusters. In this way, clusters transferred to those regions of the bare LTG:GaAs substrate were washed off while those tethered to the XYL SAM remained on the LTG:GaAs substrate.

The resulting structure of a patterned array of Au nanoclusters on LTG:GaAs (Fig. 8.6) was imaged using SEM, as shown in Fig. 8.8. (This image was taken by David Janes in School of Electrical and Computer Engineering, Purdue University.) In this image, the light regions are bare LTG:GaAs substrate (without cluster arrays) and the dark regions are covered by Au nanocluster arrays. The contrast between the two types of regions indicates that the use of patterned tether regions has resulted in deposition of Au nanocluster arrays primarily within the selected regions. The lines and cells illustrated in this pattern represent two important structures for defining computational structures and the interconnections between such cells. The width of the patterned lines are ~ 3 microns, but both the stamp pad patterning of XYL tether molecule and the deposition of nanocluster arrays on the surface should be applicable to patterns with deep submicron dimensions.

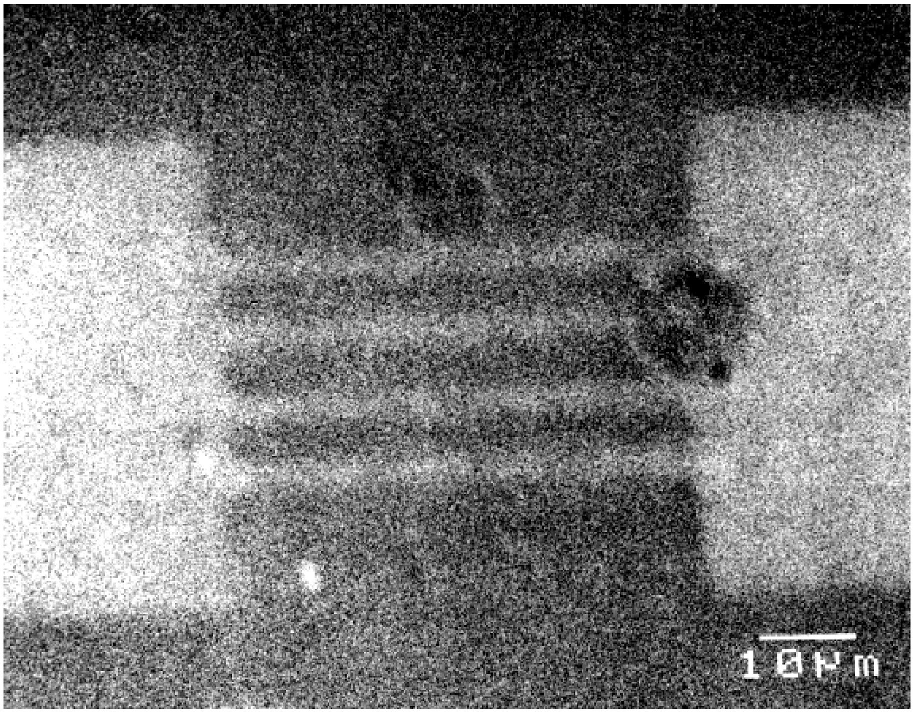


Figure 8.8

A SEM micrograph of a patterned 2-D Au nanocluster array on LTG:GaAs. The light colored regions are bare LTG:GaAs substrate and the dark colored regions are covered by the Au nanocluster array.

The stability of these patterned regions was investigated using UHV STM. When STM tip was over the Au nanocluster array, hexagonal close-packed ordering was observed, as shown in Fig. 8.9. In STM images obtained with smaller scan sizes, the hexagonal facets of individual Au clusters were clearly visible, as shown in Fig. 8.10. In addition, the height variation in such images was small, indicating the presence of a highly correlated monolayer of Au clusters. The well-defined, stable images verify that ordered arrays were transferred to the XYL-coated regions on the LTG:GaAs surface and that the clusters are well tethered mechanically to the surface. Although the limited scan size of a high resolution STM scan ($\sim 0.1\ \mu$m) and the inability to controllably move the stage in micron-scale steps prevents simultaneous observation of the nanometer scale cluster features and the lithographically defined pattern, the observations at various locations are consistent with the interpretation that the array has been selectively deposited in the XYL-coated regions. In scans at arbitrary positions on the LTG:GaAs surface, STM imaging revealed either (i) a close-packed arrays of clusters or (ii) no evidence of clusters or cluster arrays. These two types of regions are believed to correspond to scans over the dark and light regions of Fig. 8.8, respectively.

The guided self-assembly technique used in this section can be applied to an ohmic contact structured GaAs substrate. Furthermore, as discussed in the previous section, it is possible to control the cluster-to-cluster resistance within an array of Au nanoclusters by a linking molecule.[18] Therefore, the guided self-assembly technique used to fabricate these patterned nanostructures has the potential to

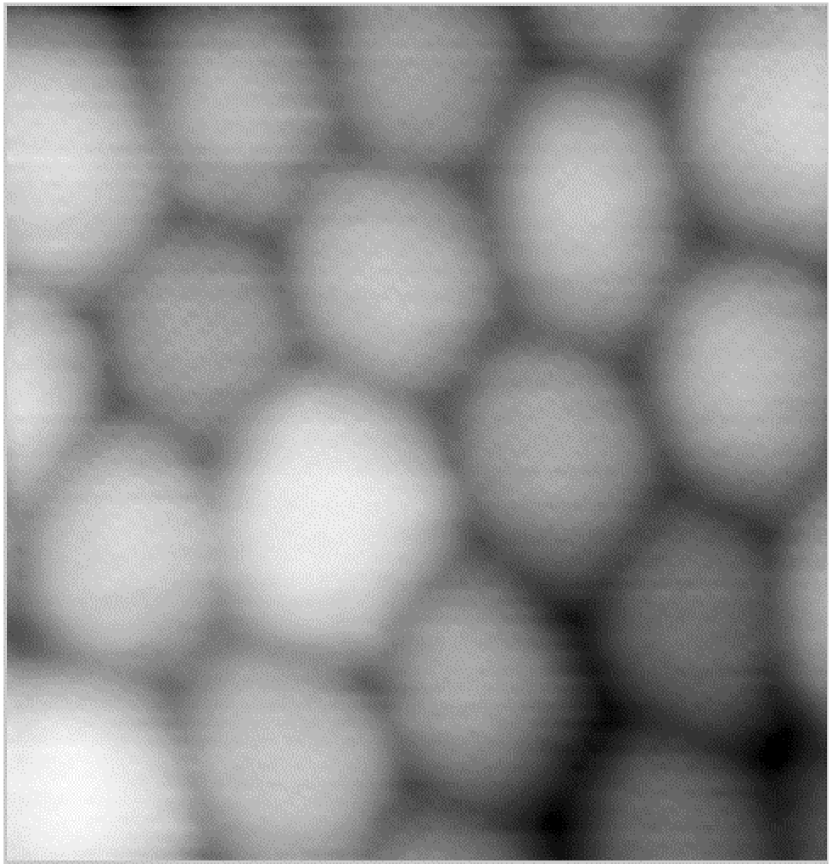


Figure 8.9

A 30 nm × 30 nm UHV STM topographic image of a hexagonal close-packed Au nanocluster array located in a XYL defined region on LTG:GaAs, illustrating that the local ordering has been preserved upon transfer to the patterned LTG:GaAs surface. The image was taken with I_{set} = 200 pA and V_{set} = -1.5 V.

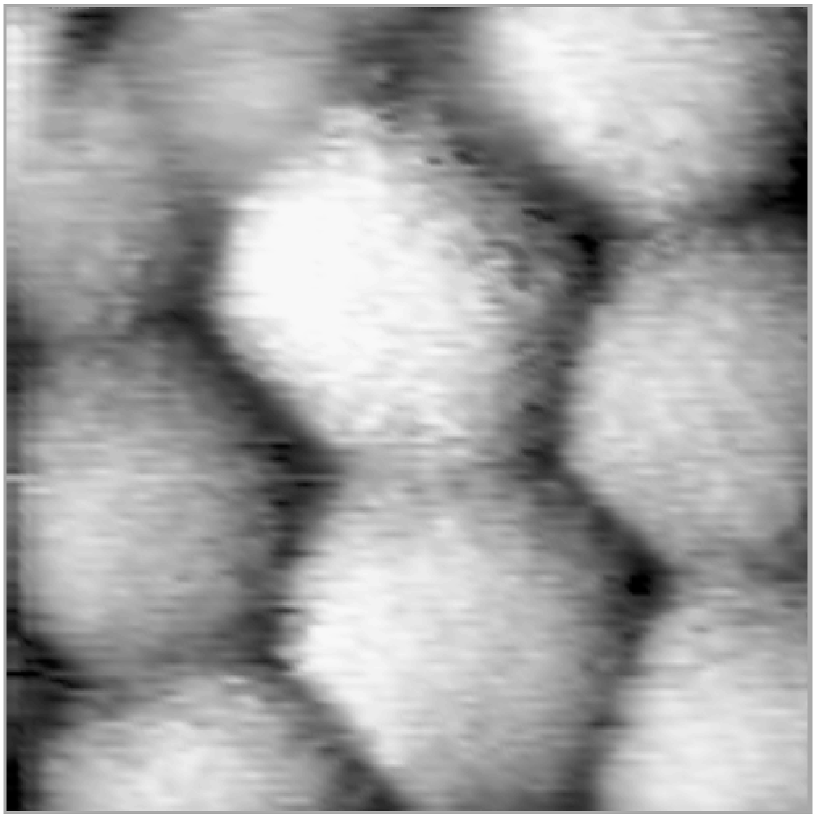


Figure 8.10

A 17 nm × 17 nm UHV STM topographic image of close-packed 2-D array of Au nanoclusters tethered to the XYL-coated Be-doped LTG:GaAs, acquired with V_{set} = -1.5 V and I_{set} = 0.15 nA. The high resolution image indicates the faceted geometry of clusters.

provide high-throughput fabrication of structures for future nanoelectronics and other nanoscale applications.

9. CONCLUSIONS

Self-assembled metal/molecule/semiconductor nanostructures were utilized to define semiconductor device and contact structures and were characterized using UHV STM.

As examples of nanoscale structures for nanoelectronic device applications, non-alloyed ohmic contact nanostructures were fabricated on LTG:GaAs as a chemically stable semiconductor surface. The controlled-geometry nanocontact was obtained by depositing a 4 nm diameter single crystalline Au cluster (truncated octahedral shape) onto the LTG:GaAs based ohmic contact structure using *ex-situ* chemical self-assembly techniques. A XYL SAM was employed on LTG:GaAs. This molecular layer forms an effective organic metal/semiconductor interface and provides both a robust mechanical tethering and a strong electronic coupling between the Au nanoclusters and the LTG:GaAs surface. The ohmic nanocontacts were attempted to n-GaAs(100) having undoped LTG:GaAs (n-type) and Be-doped LTG:GaAs (still n-type) cap layers. STM and spectroscopic studies have indicated that the nanocontacts are stable and have ohmic contact behaviors, regardless of the dopant type of LTG:GaAs cap layer. When an undoped LTG:GaAs cap layer is used for the ohmic nanocontacts, a specific contact resistance of 1×10^{-6} $\Omega\cdot\mathrm{cm}^2$ and a current density of 1×10^6 A/cm^2 have been measured from STM. For the case of the nanocontacts on a Be-doped LTG:GaAs cap layer, the corresponding values are 1×10^{-7} Ω·cm^2 and 1×10^7 A/cm^2, respectively. The ohmic nanocontact is mainly due to the sequential tunneling through the XYL layer and the LTG:GaAs layer while a midgap band of defect states (midgap states) in the LTG:GaAs layer assists conduction as if it effectively reduces the barrier width. Improved surface stability as evidenced by a lower oxidation rate and conduction through the large amount of the midgap states distributed around the Fermi level in Be-doped LTG:GaAs provide a natural explanation for the higher quality ohmic contact properties of the nanocontact to the Be-doped LTG:GaAs cap layer.

Another interesting approach was to combine the nanoscale elements (Au nanoclusters) and ordering from self-assembly processes with a procedure which can impose a somewhat arbitrary larger-scale pattern to form the specific configurations and interconnections needed for computation. Toward this goal, high-quality hexagonal close-packed arrays of Au nanoclusters ($\sim$ 5 nm in diameter) were formed within patterned regions on active GaAs substrates employing LTG:GaAs cap layer and were characterized using STM. The approach utilizes a patterned template which guides the self-assembled elements into pre-selected regions with a molecular tether (XYL). The local ordering at the nanometer scale is provided by a chemically driven self-assembly process, while the arbitrary global pattern is defined by the patterned template with a soft lithographic technique. The directed self-assembly techniques used to fabricate these structures have the potential to provide high-throughput fabrication of structures for nanoelectronics and other nanoscale applications.

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APPENDICES

Appendix A: Schematics of Sample Holder

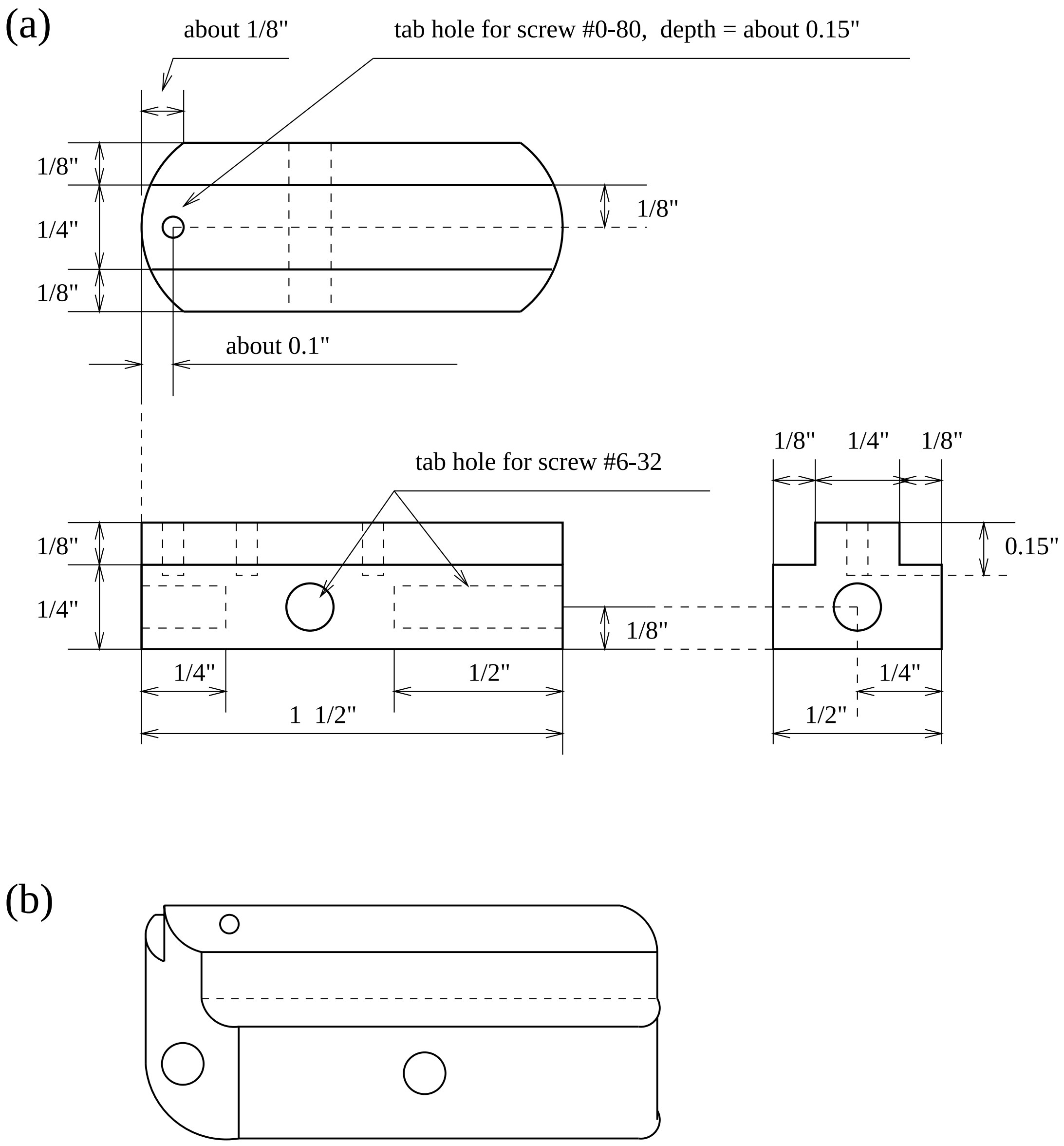

Figure A.1

Schematics of custom designed sample holder (material: Al) for STM experiment. (a) 2-D schematics. (b) 3-D schematics.

Appendix B: Schematics of Tip Holder

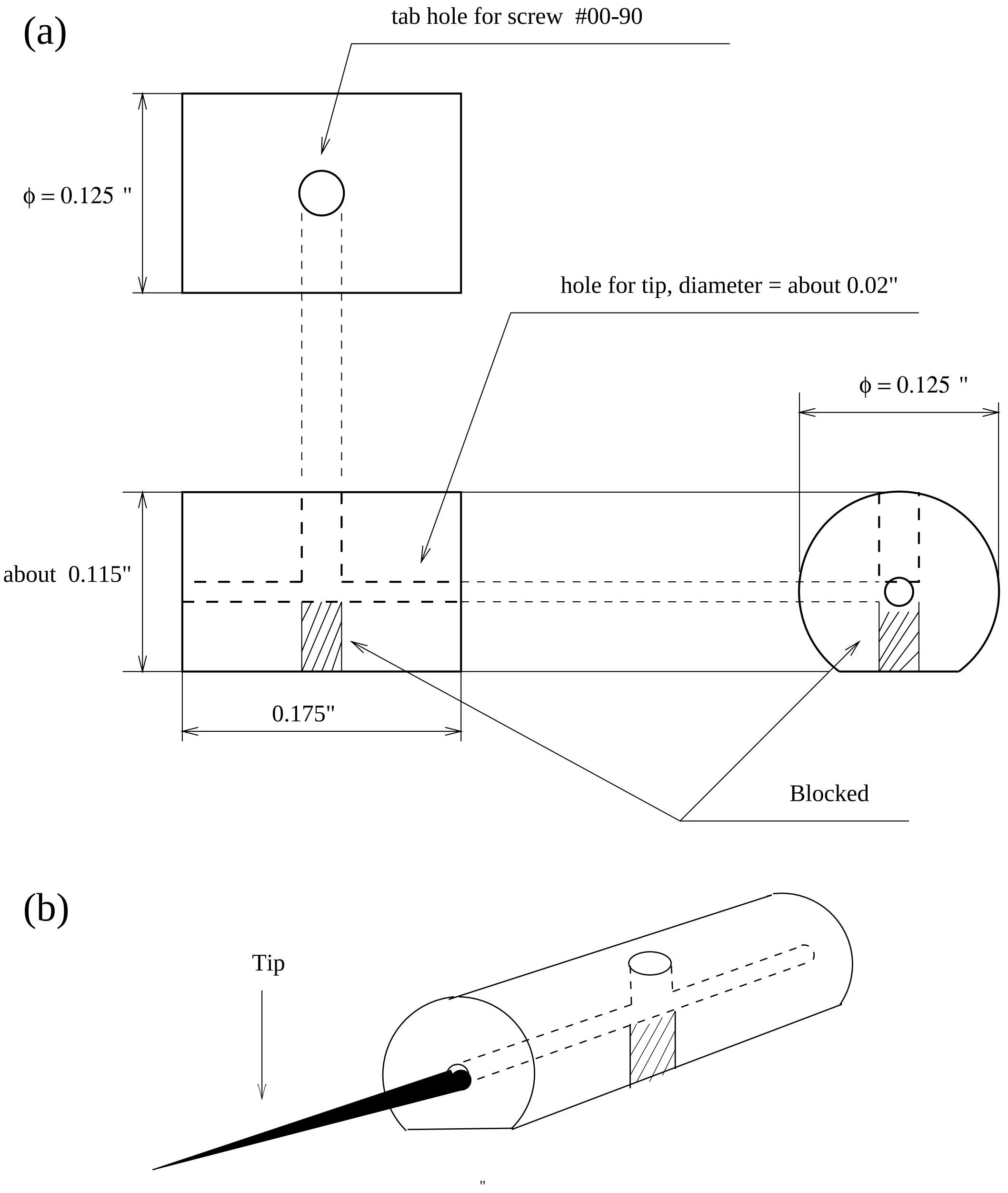

Figure B.1

Schematics of custom designed tip holder (material: stainless still) for STM experiment. (a) 2-D schematics. (b) 3-D schematics.

Appendix C: Schematics of Tip Transfer Kit

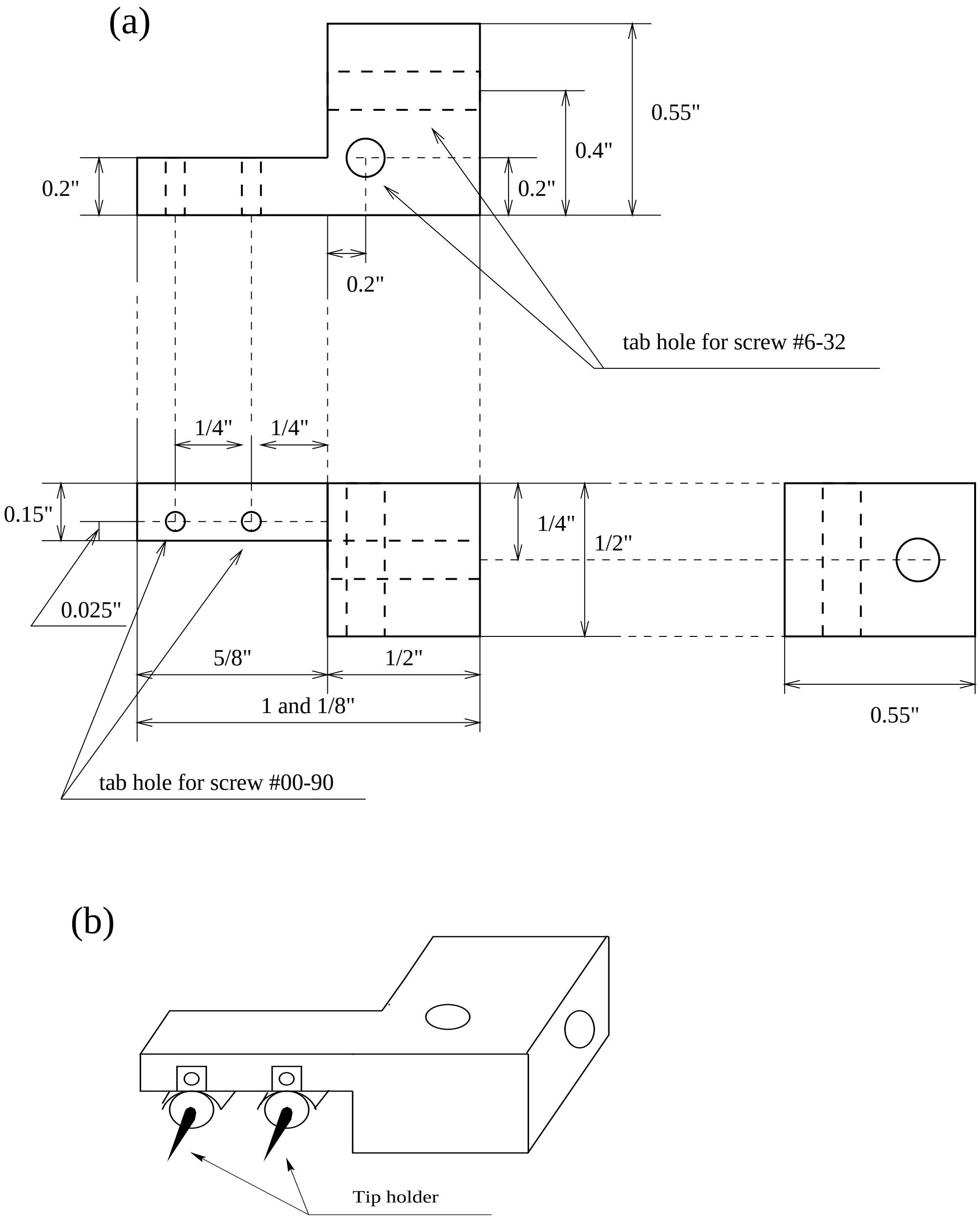

Figure C.1

Schematics of custom designed tip transfer kit (material: Al) for STM experiment. (a) 2-D schematics. (b) 3-D schematics.

Appendix D: ADEPT Simulation Input Files

These are the input files for energy band calculation of ohmic contact structured GaAs layers in ADEPT simulation.

I acknowledge Nien-Po Chen in Department of Physics, Purdue University for providing the input files.

Simulation Hub: <http://punch.ecn.purdue.edu/>[109]

[ADEPT Input file for undoped LTG:GaAs/n++ GaAs layers]

```
* title LTG:n++ GaAs
* title LTG:GaAs | n++GaAs at 300 K
mesh nx=250
misc tempk=300
$ set boundary conditions......phib = 0.3 or 0.7 eV (for wdfrt)
bc mbc=4 wdfrt=0.3 spf=1e7 snf=1e7 spb=1e7 snb=1e7
$ specify properties of undoped LTG GaAs layer
* layer n LTG GaAs
layer t=30 eg=1.422 chi=4 nc=4.7e17 nv=1.5e19 ks=13
+ un=47.84 up=25.97
+ ntt.shr=1e20/-4.5e18 et.shr=-.2/-.6
+ sig.shr=.25/.2 taun.shr=1e-8/1e-8 taup.shr=1e-8/1e-8
$ specify properties of the n++ GaAs layer
* layer n++ GaAs doped with Si n=5e19
layer t=500 nd=1e20 gd=2 ead=0.0058 un=170.6 up=2.485
+ eg=1.422 chi=4 nc=4.7e17 nv=1.5e19 ks=13
$ compute equilibrium solution
i-v v=0
solve itmax=50 delmax=1e-6
output info=3 copies=1
```

[ADEPT Input file for XYL/undoped LTG:GaAs/n++ GaAs layers]

```
* title XYL, LTG and n++ GaAs
mesh nx=250
$ set boundary conditions for wdfrt
bc mbc=4 wdfrt=2.0 spf=1e7 snf=1e7 spb=1e7 snb=1e7
* layer XYL
layer t=10 eg=3.6 chi=2.6 nc=2.5e19 nv=2.5e19 ks=2.25
+ un=47.84 up=25.97
* layer LTG GaAs (undoped)
layer t=80 eg=1.42 chi=4 nc=4.7e17 nv=1.5e19 ks=13
+ un=47.84 up=25.97
+ ntt.shr=1e20/-4.5e18 et.shr=-.2/-.6
+ sig.shr=.25/.2 taun.shr=1e-8/1e-8 taup.shr=1e-8/1e-8
* layer n++ GaAs doped with Si n=5e19
layer t=1000 eg=1.42 chi=4 nc=4.7e17 nv=1.5e19 ks=13
+ un=250.4 up=4.938
+ nd=5e19 gd=2 ead=.0058
$ compute equilibrium solution
i-v v=0
solve itmax=50 delmax=1e-6
output info=3 copies=1
```

[ADEPT Input file for XYL/Be-doped LTG:GaAs/n++ GaAs layers]

```
* title XYL, LTG and n++ GaAs

mesh nx=250

$ set boundary conditions for wdfrt

bc mbc=4 wdfrt=2.0 spf=1e7 snf=1e7 spb=1e7 snb=1e7

* layer XYL

layer t=10 eg=3.6 chi=2.6 nc=2.5e19 nv=2.5e19 ks=2.25

+ un=47.84 up=25.97

* layer LTG GaAs (Be-doped)

layer t=80 eg=1.42 chi=4 nc=4.7e17 nv=1.5e19 ks=13

+ un=47.84 up=25.97

+ ntt.shr=1e20/-4.5e18 et.shr=-.2/-.6

+ sig.shr=.25/.2 taun.shr=1e-8/1e-8 taup.shr=1e-8/1e-8

+ na=1e20 ga=4 eaa=0.028

* layer n++ GaAs doped with Si n=5e19

layer t=1000 eg=1.42 chi=4 nc=4.7e17 nv=1.5e19 ks=13

+ un=250.4 up=4.938

+ nd=5e19 gd=2 ead=.0058

$ compute equilibrium solution

i-v v=0

solve itmax=50 delmax=1e-6

output info=3 copies=1
```

Appendix E: MolecularIV Simulation Input File

This is the input file for XYL molecule in MolecularIV simulation.

First Column is atomic number and second, third, and fourth column are x, y, and z coordinate of XYL molecule. The coordinates of XYL molecule can be obtained using HyperChem program.

I acknowledge Ferdows Zahid in School of Electrical and Computer Engineering, Purdue University for providing the input file.

Simulation Hub: <http://punch.ecn.purdue.edu/>[118]

[MolecularIV Input file for XYL]

```
6      1.19886    -3.62500     0.00000
6      1.19897    -2.22921    -0.00166
6     -0.00072    -1.51017     0.00386
6     -1.20023    -2.22913     0.01892
6     -1.19998    -3.62507     0.02125
6     -0.00058    -4.34470     0.01154
6      0.00000    -5.85502     0.00000
6      0.00000     0.00000     0.00000
16     0.01629     0.58751    -1.72691
1      2.16131    -4.16310    -0.00805
1      2.16068    -1.69018    -0.01485
1     -2.16228    -1.69056     0.02203
1     -2.16259    -4.16279     0.03034
1      0.87603    -6.22771    -0.57869
1     -0.90791    -6.23086    -0.52516
1     -0.89704     0.38237     0.53834
1      0.88786     0.37953     0.55532
16     0.05144    -6.46726     1.71680
```

Appendix F: MATLAB Programs for Ohmic Nanocontact Conduction Model

This is a MATLAB program to calculate the specific contact resistance versus the barrier width of LTG:GaAs.

```
% begin the MATLAB program.
% parameters
h=6.626E-34; % (J sec)
h_bar=1.054E-34; % (J sec)
w1=9.0E-10; % (m) barrier width of XYL as a rectangular barrier
m=9.11E-31; % free electron mass (Kg)
m_eff=6.1037E-32; % (Kg) Effective electron mass in GaAs = 0.067 × m_electron
e=1.6E-19; % (C) electron charge
phi_b1_eV=2.0; % (eV) barrier height in XYL
phi_b1=phi_b1_eV*e; % (J) barrier height in XYL
phi_b2_eV=0.35; % (eV) barrier height in LTG:GaAs
phi_b2=phi_b2_eV*e; % (J) barrier height in LTG:GaAs
kT=26E-3; % (eV) thermal energy at room temperature
pi=3.141592;

% be ready to write output file with file name of “output”.
fid=fopen(’output’, ’w’);
fprintf(fid,’w\t r_c\t r_c2\n’); % column title
```

```
for j=1:1:10 % for the barrier width loop
    w(j)=j*1E-9; % convert barrier width into meter unit.
    w_nm(j)=j; % barrier width in nanometer unit
    for i=1:1:350 % for the integration loop
    % 350 represent barrier height 0.35 eV.
        E(i)=(i-1)*0.001; % for the integration from 0 to 0.349 eV
        T1=exp(-2*w1/h_bar*sqrt(m*(phi_b1-E(i)*e)));
        % transmission function for rectangular barrier
        % use T1 = 0.006 for transmission function for XYL.
        T2(j)=exp(-4*w(j)/(3*phi_b2*h_bar)*sqrt(2*m_eff)*(phi_b2-E(i)*e)^1.5);
        % transmission function for LTG:GaAs
        f(i)=T1*T2(j)/(1+exp(E(i)/kT));
        f2(i)=T2(j)/(1+exp(E(i)/kT));
        % overall expression of the function in the integration
    end % for i loop
    area=trapz(E,f)*e; % integration
    area2=trapz(E,f2)*e; % integration
    r_c(j)=1.0/(4*pi*m*e*e/h^3*area)*10000;
    r_c2(j)=1.0/(4*pi*m*e*e/h^3*area2)*10000;
    % r_c expression in ohm cm^2 unit
fprintf(fid,’%.5e\t%.5e\t%.5e\n’, w_nm(j), r_c(j), r_c2(j));
```

```
% write w_nm, r_c, and r_c2 in the output file as ASCII.
end % for j loop

% plot
semilogy(w_nm,r_c) % log plot of r_c versus w
% or semilogy(w_nm,r_c2) % log plot of r_c2 versus w
xlabel('Barrier Width (nm)')
ylabel('Contact Resistance (Ohm cm^2)')
% axis([0 10 1E-7 1E-4])

% be ready to close the output file.
fclose(fid);
% end the MATLAB program.
```

This is a MATLAB program to calculate current density versus voltage using the sequential tunneling conduction model on the nanocontact structure (Au cluster/XYL/LTG:GaAs).

```
% begin the MATLAB program.
% parameters
h=6.626E-34; % (J sec)
h_bar=1.054E-34; % (J sec)
m=9.11E-31; % free electron mass (Kg)
m_eff=6.1037E-32; % (Kg) Effective electron mass in GaAs = 0.067 × m_electron
w=6.0E-9; % (m) barrier width of LTG:GaAs as a triangular barrier
e=1.6E-19; % (C) electron charge
phi_b_eV=0.35; % (eV) barrier height in LTG:GaAs
phi_b=phi_b_eV*e; % (J) barrier height
kT=26E-3; % (eV) thermal energy at room temperature
kT_J=4.146E-21; % (J) thermal energy at room temperature
pi=3.141592;

% be ready to write output file with file name of “output”.
fid=fopen(’output’, ’w’);
fprintf(fid,’V\t J1\t J2\n’); % column title
```

```
for j=1:1:21 % for the voltage loop
    V(j)=(j-1)*0.01; % voltage from 0 to 0.2 V
    for i=1:1:(j*10+340) % for the integration loop
    % integration up to eV + phi_b (0.2 + 0.349 eV)
        E(i)=(i-1)*0.001;
        T1=0.006;
        % transmission of XYL at Fermi level between Au contacts
        T2(j)=exp(-4*w/(3*phi_b*h_bar)*sqrt((2*m_eff)/(1+(V(j)*e/phi_b)))*
                ((phi_b+V(j)*e-E(i)*e)^1.5));
        % transmission function for LTG:GaAs
        N(i)=log((1+exp((-E(i)+V(j))/kT))/(1+exp(-E(i)/kT)));
        % from integrating Fermi-Dirac functions
        TN1(j)=T1*N(i);
        TN2(j)=T2(j)*N(i);
        % overall expression of the function in the integration
    end % for i loop
    area1=trapz(E,TN1)*e; % integration
    area2=trapz(E,TN2)*e; % integration
    J1(j)=(4*pi*m*e/h^3)*kT_J*area1/10000;
    J2(j)=(4*pi*m*e/h^3)*kT_J*area2/10000;
    % J, current density in A/cm^2 unit
fprintf(fid,'%.5e\t%.5e\t%.5e\n', V(j), J1(j), J2(j));
```

```
% write V, J1, and J2 in the output file as ASCII.
end % for j loop

% plot
plot(V,J1) % or plot(V,J2)
xlabel(’Voltage (V)’)
ylabel(’Current Density (A/cm^2)’)

% be ready to close the output file.
fclose(fid);
% end the MATLAB program.
```

Appendix G: Acronym

SAM: Self-assembled monolayer

DDT: Dodecanethiol, $CH_3(CH_2)_{11}SH$

ODT: Octadecanethiol, $CH_3(CH_2)_{17}SH$

XYL: Xylyl dithiol, $HS\text{-}CH_2\text{-}C_6H_4\text{-}CH_2\text{-}SH$

HOMO: Highest occupied molecular orbital

LUMO: Lowest unoccupied molecular orbital

PDMS: Polydimethylsiloxane

DOS: Density of state

LTG:GaAs: GaAs grown at a low temperature

HOPG: Highly oriented pyrolitic graphite

MBE: Molecular beam epitaxy

UHV: Ultra high vacuum

DSP: Digital signal processor

ADC: Analog-to-digital converter

DAC: Digital-to-analog converter

STM: Scanning tunneling microscopy

STS: Scanning tunneling spectroscopy

CITS: Current imaging tunneling spectroscopy

AFM: Atomic force microscopy

SEM: Scanning electron microscopy

TEM: Transmission electron microscopy

XPS: X-ray photoemission microscopy

UPS: Ultraviolet photoemission spectroscopy

LEED: Low-energy electron diffraction

RMS: Root mean square

SET: Single electron tunneling

M-S: Metal-semiconductor

M-I-S: Metal-insulator-semiconductor

VITA

VITA

Takhee Lee was born in Taegu, Korea on November 12, 1969. He lived in Taegu until high school, then he moved to Seoul in Korea to start his college life. He received Bachelor's and Master's degree in physics, at Seoul National University, Seoul in Korea in 1992 and 1994, respectively. Then, He attended Purdue University to start his Ph. D. study in physics in 1995. While study in physics at Purdue University, he got married with Kwihyun Nam.