Appropriate DC operating conditions must be established for any circuit before it can be used to respond to an input signal. These are called the bias or quiescent conditions (i.e., without an input signal). The quiescent currents and voltages in the circuit must permit the expected changes to occur without getting the transistor out of its normal operating range.

This experiment involves only DC measurements, however we still use bypass capacitors because AC signals can distort DC measurements. Refer to GIL sections 3.2 and 13.1 for further instructions. Remember to turn off the voltage supplies before components are changed.

A. Theoretical Summary

The quiescent drain voltage \((V_d)\) determines the maximum possible change in drain voltage. \(V_d\) cannot go higher than \(V_p\) or lower than the minimum voltage needed to operate the FET.

The minimum voltage is equal to \(V_T\) because the gate is at zero volts in this circuit, recall that \(I_d = (V_p - V_T)/2R_3\). The two following equations express the maximum possible drain variations are \(+\Delta V_d \leq (V_p - V_d)\) and \(-\Delta V_d \leq (V_d - V_T)\).

These limits restrict the amplitude of the output signal, \(V_o\). The value of \(V_d\) is determined by the voltage drop across \(R_3\)

\[
V_d = V_p - I_d R_3
\]  
(1.1)
The maximum amplitude is obtained for a sine wave when the positive and negative limits are equal. \( I_d \) is then given by the following relation:

\[
I_d = \frac{(V_p - V_r)}{2R_3}
\]  

(1.2)

1. **Self-Bias for a FET**, \( V_n = 0 \). The value of \( R_1 \) needed to obtain the desired \( I_d \) is:

\[
R_1 = \frac{V_T}{I_d} \left[ 1 - \left( \frac{I_d}{I_{dss}} \right)^{1/2} \right]
\]  

(1.3)

2. **Controlled Biasing**, \( V_n \) is nonzero. The current is much less dependent on transistor parameters when a biasing voltage, \( V_n \), and a larger series resistor, \( R_1 \), are used. The drain current is given by

\[
I_d = \frac{(V_{gs} - V_n)}{R_1}
\]  

(1.4)

When \( V_{gs} \) is not negligible compared to \( V_n \), it can be estimated using the following equations.

\[
V_{gs} = V_T \left[ 1 - \left( \frac{I_d}{I_{dss}} \right)^{1/2} \right]
\]  

(1.5)

\[
V_{gs} \approx 0.3V_T \text{ when } I_d \approx I_{dss/2}
\]

In BJT circuits, \( V_{be} \) can usually be estimated by 0.6V, but it may be necessary to include the voltage drop across \( R_2 \). The collector current is then given by

\[
I_c = \frac{-0.6V - V_n}{R_1 + R_2 / h_{fe}}
\]  

(1.6)

When a voltage divider is used to lift the base of a BJT above common, it may be necessary to include the effect of base current to calculate the base voltage. The base voltage is then given by

\[
V_b = V_p \frac{(R_2 \parallel r_b)}{(R_4 + (R_2 \parallel r_b))}
\]  

(1.7)
\[ r_b \approx h_{fe} R_1 \]  

As usual, the BJT current is determined by the voltage across the resistor \( R_1 \) in series the emitter.

\[ I_c = \frac{(V_b - 0.6V)}{R_1} \]

The equivalent change in base-emitter voltage \((V_{be})\) due to heating in a BJT is,

\[ V_H = C_T \Delta T = C_T (\theta_{ja} \Delta P) = C_T (\theta_{ra} I_c \Delta V_c) \]

\[ C_T = 2mV/\text{degreeC} \]

When \( I_c \) is held approximately constant, by using a large value for \( R_1 \), \( V_H \) is observed as a change in \( V_{be} \). \( V_{be} \) decreases when the temperature increases.

**B. Simplified Measurement for \( I_{dss} \) and \( V_T \)**

A multi-meter can be used to measure \( I_{dss} \) and \( V_T \) easily by inserting the meter in series with the source.

The long meter lead can cause the FET to oscillate unless a by-pass capacitor is used at the source. The source voltage is determined by the FET current through the internal resistance, \( R_m \), of the meter.

\[ V_{gs} = R_m I_d \leq V_T \]

The source voltage cannot be larger than \( V_T \) because that is the value that reduces \( I_d \) to zero. When the meter is set to read voltage, \( R_m \) is very high, hence \( I_d \) will be very small, which means that the meter reading will be approximately equal to \( V_T \).

\[ V_{meter} = V_{sg} = 0.9V_T \text{ Meter on voltage scale} \]
A 10% correction is included because $I_d$ is slightly larger than zero. $R_m$ is very small when the meter is on the current scale, hence $V_{gs}$ is approximately zero, which means that $I_d = I_{dss}$.

$$I_{\text{meter}} = I_d = I_{dss} \quad \text{Meter on current scale}$$

This is a very useful procedure, because the basic FET parameters can be measured using only a voltage source and a V-I meter. (A 9V battery will do if you don’t have a power supply available)

**1 - Use this procedure to measure $V_T$ and $I_{dss}$ for a FET. Use the power supply for the drain voltage.**

**C. Self-Biasing of a JFET**

Typical values and data from the device specifications for $V_T$ and $I_{dss}$ will be used to calculate bias conditions for homework. The measured values of these parameters from step 1 will be used to calculate observables in lab.

**2 - Use the typical $V_T$ and $I_{dss}$ given on the component sheet. Calculate the $I_d$ needed to set the quiescent drain voltage ($V_d$) half way between the power supply voltage ($V_p$) and the minimum voltage ($V_m$) needed by FET. ($V_m = V_T$ in this circuit because $V_{gs} = 0$)**

Use equation (1.4) to calculate the $R_1$ needed to obtain this $I_d$. Calculate the maximum amplitude (peak-peak), undistorted sine wave that could be obtained at the drain. Include these calculations in your laboratory report.

**3 - Use the measured values from step 1 in the process described in step 2 to calculate $R_1$. Use equation (1.5) to calculate the expected $V_s$. Use the resistor value**
for $R_1$ that is closest to the calculated value. Measure $V_d$ and $V_s$ and compare to that expected.

D. Controlled FET Biasing

Better control of $I_d$ can be obtained by connecting the lower end of $R_1$ to a negative power supply ($V_n$) rather than to ground. (The gate stays connected to ground.) In this arrangement $I_d$ is controlled primarily by $V_n$ and $R_1$, but the extremes of $V_T - I_{ds}$ must be considered unless $V_n$ is much greater than $V_T$.

4 - Include in your laboratory report the following calculations. This circuit should have the same $I_d$ and $V_d$ as step 2. Use the same typical $V_T$ and $I_{ds}$. Use eqn. (1.5) to calculate $V_{gs}$. Also calculate $R_1$.

Next we will see what effect different FET parameters would have on the quiescent conditions. Calculate $I_d$ and $V_d$ if the FET had the maximum $V_T$ and $I_{ds}$ given in the spec sheet. Use the $I_d$ obtained with typical parameters in the first part of this problem as an estimate for the new $I_d$ in eqn. (1.5), which in turn is used to estimate the new $V_{gs}$. This estimate is adequate because $R_1$ prevents $I_d$ from changing dramatically. Repeat for the minimum parameters given in the spec sheet. When $V_n \gg V_{gs}$, $I_d$ is relatively independent of the FET parameters because they only affect $V_{gs}$.

5 - Use a 5% resistor that is nearest to the value of $R_1$ calculated in step 4. $V_s$ will be approximately the same as that calculated in step 3 because the circuit is designed to have the same $I_d$. Measure $V_d$ and $V_s$ and compare to the expected values.
6 - Observe $V_s$ with a meter while you vary $V_n$ from 0 to 25 volts. You will see that $V_s$ changes as necessary so that the channel can conduct the current flowing through $R_1$. Give a brief explanation of how this self-adjustment occurs in your own words.

7 - Include in your laboratory report the following calculations. The object is to set the quiescent $V_d$ to obtain a maximum positive change at the drain i.e. $V_d$ is a positive pulse. $I_d$ should be selected so that $V_d = V_T$ (max). Then in the worst case there will be adequate drain voltage for the FET. Next calculate $R_1$ estimating $V_{sg} = V_T$ (max). What value of $I_d$ would occur with this $R_1$ if $V_T$ and $I_{dss}$ were at the minimum? What limit would be imposed on the amplitude of $V_d$? No measurement required.

E. Controlled BJT Biasing

Although the circuit used here is similar to that in the preceding section, remember that the pin order on the BJT and FET are not the same. First, a small $R_2$ will be used so that it doesn’t affect the measurement. Then $R_2$ will be larger so that it has an effect.

8 – Using the specified parameters in step 8

calculate $I_e$, $I_c$, $I_b$, $V_b$, and $V_c$, include these

in your laboratory report.

9 – Change the value of $R_2$ and repeat these calculations.

10 - Use the digital meter to measure the voltages specifies in steps 8 and 9.

F. Controlled BJT Biasing with a Voltage Divider
The advantage of controlled biasing can be obtained with a single power supply by using a voltage divider to set the DC voltage at the input. The calculations are simple for a FET because its gate current is negligible, but the base current of a BJT can affect the divider. First we consider a case where the divider resistors are small, divider current large, so that $I_b$ can be neglected. Next we increase the divider resistors to obtain a higher resistance at the input and include the effect of $I_b$ on $V_b$.

11 - Calculate $V_b$, $I_c$, and $V_c$ and include these in your laboratory report. What is the maximum positive and negative change available at the collector? (Assume an AC ground at the emitter).
12 - Repeat 11 for a different divider resistances.
13 - Set up the circuits and use the digital meter to measure the voltages specified in steps 11 and 12. An emitter bypass capacitor is not needed for these DC measurements.
2-3. $V_p = 20V$, $V_T = 2V$, $I_{DSS} = 8\, \text{ma}$, $R_3 = 10\, \text{K}$
4-7. $V_p = 20V$, $V_n = -20V$, $R_3 = 10\, \text{K}$
8-10. $V_p = 20V$, $V_n = -20V$, $R_3 = 10\, \text{K}$, $R_1 = 20\, \text{K}$, $h_{fe} = 100$
8. $R_2 = 4.7\, \text{K}$
9. $R_2 = 510\, \text{K}$
11-13. $V_p = 25V$, $R_1 = 3.3\, \text{K}$, $R_3 = 20\, \text{K}$, $h_{fe} = 100$
11. $R_2 = 3.9\, \text{K}$   $R_4 = 20\, \text{K}$
12. $R_2 = 33\, \text{K}$   $R_4 = 150\, \text{K}$