Physics 536 - Assignment #9

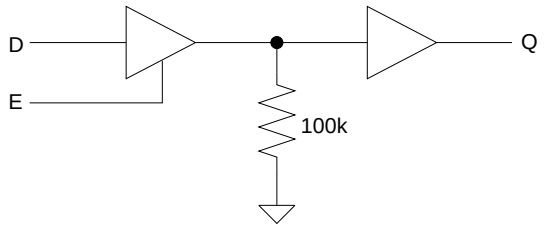
1. (a) Using discrete logic gates, draw the schematic design for a 4-1 de-multiplexor circuit, which produces the following truth table:

D_3	D_2	D_1	D_0	S_1	S_0	Q
$\times$	$\times$	$\times$	y	0	0	y
$\times$	$\times$	y	$\times$	0	1	y
$\times$	y	$\times$	$\times$	1	0	y
y	$\times$	$\times$	$\times$	1	1	y

where $\times$ indicates "don't care". Label any intermediate logic states used in the schematic circuit. Feel free to use AND and OR gates with an arbitrary number of inputs and with bubbles at any convenient place to indicate inversion of a signal.

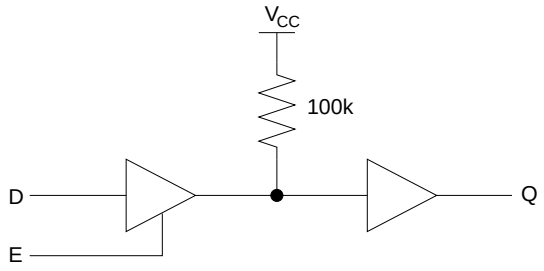
(b) Show how the same truth table could be implemented using 2-input logic gates and tri-state buffers.

2. (a) Consider the following circuit, in which the output of a TTL tri-state buffer is enabled by E:

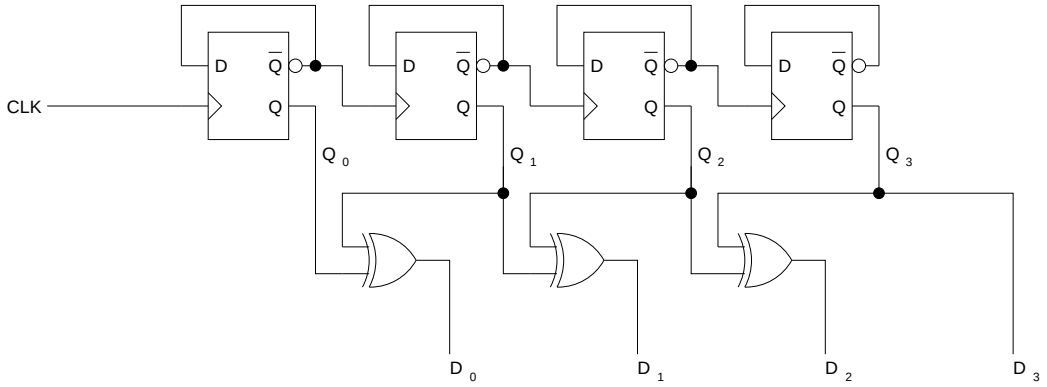


Write the truth table for Q as a function of D and E. What boolean algebraic operation does this implement?

(b) Write the truth table for the following circuit and express Q as a function of D and E.



3. (a) The *Grey code* is a method for representing integers such that the representations of integers i and $i+1$ have exactly one bit that is different. Complete the truth table for the following Grey code counter circuit for 16 clock cycles:



i	CLK	Q_3	Q_2	Q_1	Q_0	D_3	D_2	D_1	D_0
0	⌠	0	0	0	0	0	0	0	0
1	⌠	0	0	0	1	0	0	0	1
2	⌠	0	0	1	0	0	0	1	1
⋮									

(b) Does the output, $D_{3\ldots0}$, have the *instantaneous* value of 0000 only once or more than once for every 16 input clock cycles? Explain why.

(c) Explain how the following circuit works and why it does not suffer from the problem that you should have identified in part (b).