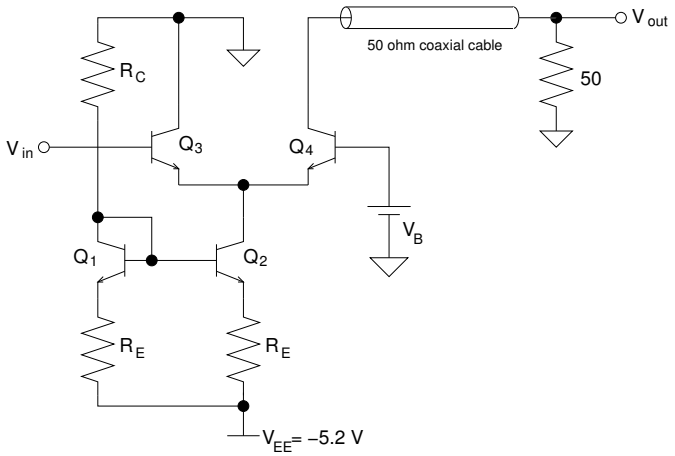
Physics 536 - Assignment #9 - Due April 21th

1. Two high-speed digital logic familes are ECL (Emittor Coupled Logic) and NIM (Nuclear Insturmentation Module) which have nominal logic levels defined as follows:

Logic level	ECL	NIM
0	-0.9 V	0 V
1	-1.8 V	-0.8 V

Describe the operation of the following circuit, which translates an ECL logic level at $v_{\rm in}$ to a NIM logic level, driven on a coaxial cable that is terminated by at 50 Ω resistor to produce $v_{\rm out}$.



(a) What current needs to flow through the 50 ohm load that terminates the coaxial cable to produce a NIM logic level of 1?
(b) What values of R_C and R_E would be needed for the current mirror to produce this current when the power supply is $V_{EE} = -5.2$ V?
(c) What values of the voltage source V_B would be needed to make the circuit operate correctly?
(d) Describe the flow of current in the circuit for both cases when $v_{\rm in} = -0.9$ V (ECL logic level 1) and when $v_{\rm in} = -1.8$ V (ECL logic level 0).

2. The truth table for an *exclusive OR* gate is

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Express the exclusive OR operation in terms of AND, OR and NOT operations both using boolean algebra and usuing symbols for logic gates.

3. The *Gray code* is a binary representation of integers in which the representation for integer $i+1$ differs from the representation of integer i by the inversion of a single bit. Thus, the 4-bit gray code representation for the integers $0 \ldots 15$ is

i	Binary	Gray code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

Design a combinatorial logic network that will translate 4-bit binary integers into their 4-bit Gray code representation.
(a) Write each bit g_0, g_1, g_2, g_3 of the Grey code representation as a boolean algebraic function of the binary digits b_0, b_1, b_2 and b_3. Simplify these expressions so that they are expressed in terms of elementary AND, OR and NOT operations.
(b) Draw a schematic representation of this translator circuit that only uses exclusive OR logic gates.
(c) Show how this circuit could be generalized to convert an arbitrary width n-bit integer to its Grey code representation.

4. Using edge-triggered D-flip-flops, design a synhronous 4-bit Gray code counter. That is, the 4-bit output of the counter, g_3, g_2, g_1, g_0, representing the integer i will synchronously switch to the representation of $i+1$ on the next rising edge of a clock signal.