



Formation of unintentional dots in small Si nanostructures

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We studied charge transport through lithographically defined Si quantum dots. At low temperatures multi-dot transport is observed. In particular, we analyzed transport through double-dot devices. The data provide compelling evidence that the extra dots are formed within the gate oxide.

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Initially, the development of single-electron devices was driven by a technological goal to create an alternative to the conventional MOSFET logic and memory circuits. As a result, silicon was the choice of the material and room temperature operation was the requirement. Indeed, several groups reported Coulomb blockade in small Si single-electron transistors [1–3] at room temperatures. Recently, a Si realization of a quantum computer has been proposed [4], and our interest in nanoscale Si devices got a new twist. This new direction has different requirements: ultra-small size and low electron density, in order to enhance quantum effects. One has to be able to precisely control the number of electrons in the dot, their spin and interaction strength. As a first step in this direction, we have shown that a small Si dot can be controllably tuned between different spin configurations by a magnetic field [5]. We note that high operating temperature is not an issue there. On the contrary, low temperature is required in order to increase the coherence time.

The low-temperature operation created a new technological challenge: most of the devices show a multi-dot transport when temperature is decreased below a few Kelvin. This behavior seems to be generic for nanoscale Si devices: even devices with no intentionally defined dot, like quantum wires [2, 3, 6, 7], point contacts [8] or short-channel devices [9], exhibit Coulomb blockade (CB). Moreover, quite often CB is observed on top of some finite conductance [8–10]. We argue that in most of these samples the appearance of the CB can be explained by the formation of an extra dot inside the oxide, thus forming a parallel channel to the wire or to the point contact. In this paper we extend our previous study of a parallel conduction channel in small Si quantum dots [11]. We present new data which unambiguously supports the conclusion that, in our samples, the extra dots are formed inside the thermally grown oxide.

We analyzed transport through small Si quantum dots fabricated from a silicon-on-insulator (SOI) wafer. The details of sample preparation were published previously in Ref. [12], and here we just outline the major steps. The top silicon layer of a SIMOX (separation by implanted oxygen) wafer is patterned by an electron-beam lithography to form a small dot, connected to wide source and drain regions, as shown in the SEM

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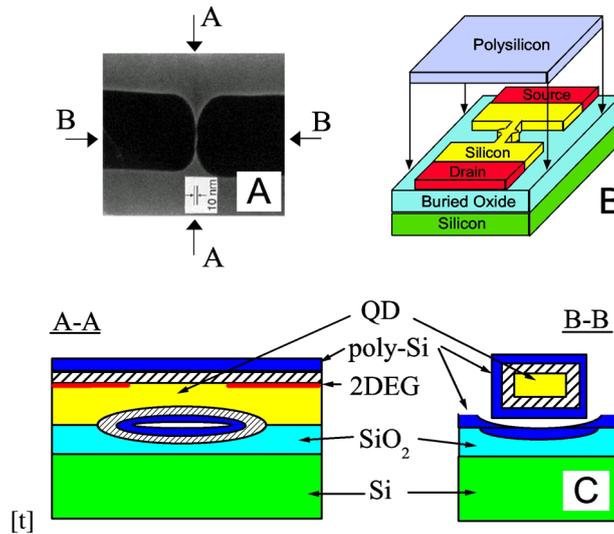


Fig. 1. A, SEM micrograph of the device; B, 3D schematic of the device structure; and C, schematic view of the device cross-section.

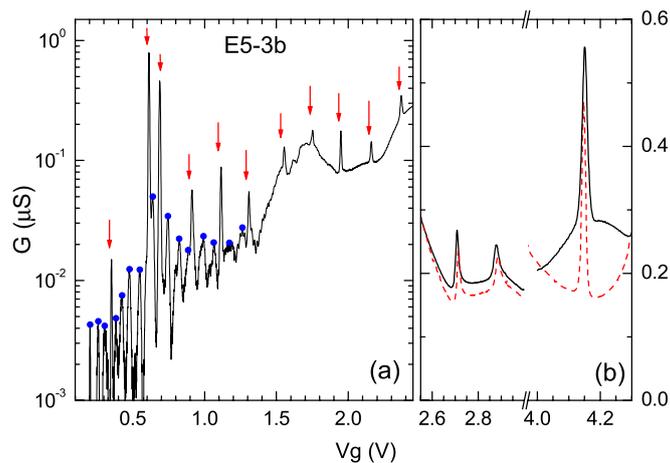


Fig. 2. Conductance as a function of gate voltage measured at $T = 1.5$ K. In A, arrows (solid dots) mark Coulomb blockade peaks through the main (extra) dot. The extra dot has finite conductance at $V_g > 1.4$ V. In B, the conductance change is shown between the two V_g sweeps: starting from zero (solid line) and after V_g was swept up to 10 V and back (dashed line).

micrograph in Fig. 1A and schematically in Fig. 1B. Some of the buried oxide is wet-etched beneath the dot transforming it into a free-standing bridge. Subsequently, 50 nm of oxide is thermally grown, which further reduces the size of the dot. Polysilicon gate is deposited over the bridge with the dot as well as over the adjacent regions of the source and drain. Finally, the uncovered regions of the source and drain are n- or p-type doped. In order to clarify the schematic of the device, the cross-section view of the device is shown in Fig. 1C along and perpendicular to the bridge. Thick lines represent a two-dimensional inversion layers which are terminated at the constrictions. The dot (QD) is formed somewhere inside the bridge and is surrounded by thermal oxide (hatched) and poly-Si gate. In this work we will present data from electron samples only, but similar data was obtained from single hole transistors as well.

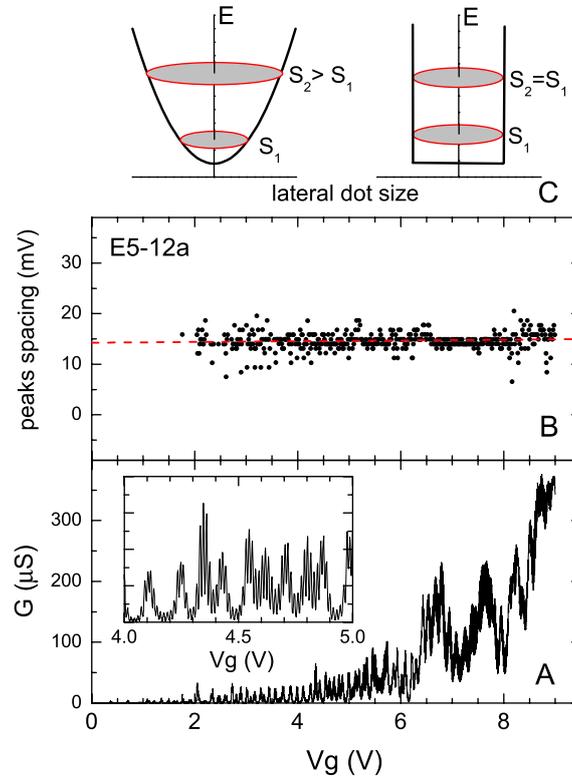


Fig. 3. A, Conductance as a function of V_g measured at $T = 3.8$ K. Modulation with $\Delta V_g \approx 100$ mV corresponds to the charging of the main dot. Oscillations with 14 mV period (charging of the extra dot) are amplified in the inset. B, Peak spacing for the extra dot is shown for 476 consecutive peaks. The dashed line is the linear fit to the data. C, The change of the dot size as the number of electrons increases is shown schematically for parabolic and hard wall potentials.

In Fig. 2 we show a low-temperature transport in one of the samples. At $T = 1.5$ K there are two sets of peaks, marked with dots and arrows in Fig. 2A. At slightly elevated temperatures $T > 10$ K only peaks, marked by arrows, survive. The average distance between these peaks is $\Delta V_g = 0.2$ V, which is consistent with the estimated gate capacitance for the lithographically defined (main) dot $C_g \approx 0.8 - 1.5$ aF ($e/C_g \approx 100-200$ mV). Moreover, as a function of the source–drain bias these peaks form Coulomb blockade diamonds with the same slopes. Thus, we conclude that the peaks, marked by arrows, originate from the main dot.

In addition, there is another set of peaks at gate voltages $V_g < 1.4$ V, marked with black dots. These peaks are spaced by 60 mV and have different bias dependence from the main dot peaks. Such peaks are the signature of a CB through some other, unintentionally formed (extra) dot. At $V_g > 1.4$ V these extra peaks disappear and the device has a finite conductance. Tunneling through the extra dot forms a parallel conduction path to the transport through the main dot. At $V_g < 1.4$ V both sets of peaks can be measured down to the lowest $T = 60$ mK. In the regime when the extra dot becomes open, $V_g > 1.4$ V, the conductance is not temperature activated in CB valleys, although peaks from the main dot remain sharp. If the dots were connected in series, most of the peaks should be exponentially suppressed at low T at $V_g < 1.4$ V (so-called ‘stochastic blockade’ [13]), while at $V_g > 1.4$ V transport should resemble CB through a single (main) dot with G being suppressed between the peaks.

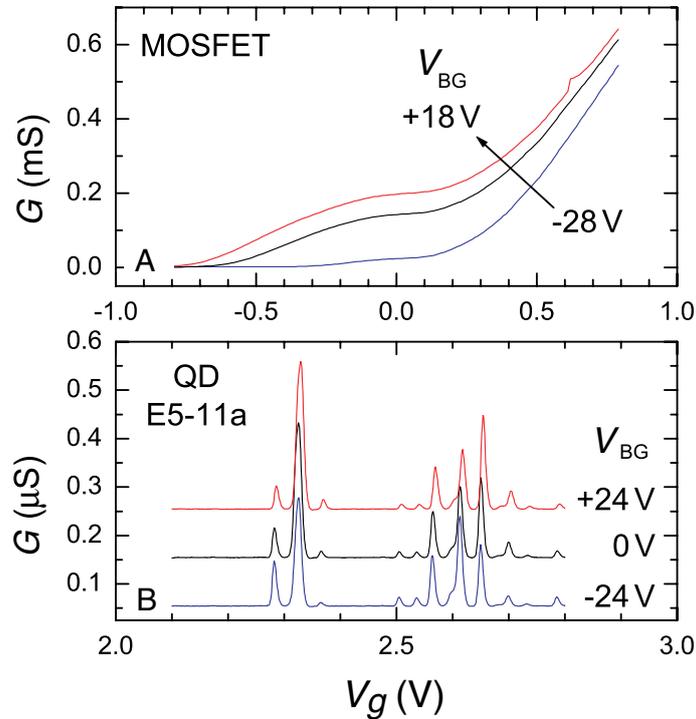


Fig. 4. A, Conductance through the MOSFET sample, nominally identical to the QD samples, without the e-beam lithography. The G changes strongly as a function of the back gate voltage. B, Conductance as a function of the front gate voltage V_g , measured at different back gate voltages V_{bg} (the curves are offset for clarity). The data were taken at $T = 4.2$ K.

There is no tunneling between the dots and the peaks from the main dot are thermally broadened down to 60 mK. The peaks remain thermally broadened even when the extra dot becomes open. An additional confirmation that conductances through the dots are added independently is presented in Fig. 2B. A wide V_g scan to 10 V changes the background conductance through the extra dot by charging some nearby impurities. The peaks from the main dot simply shift with the background, retaining their width and amplitude.

Where is the extra dot located? The period of the CB oscillations from the extra dots ranges from 10 to 60 mV, corresponding to a gate capacitance of 3–16 aF. The maximum capacitance between the gate and the dot in the bridge is 1.5 aF (estimated from the geometry of the sample). Thus, the extra dot is formed somewhere outside, although along, the Si bridge. There is strong experimental evidence that the extra dot is formed inside the oxide. Some samples show a huge number of CB oscillations through the extra dots. For the sample shown in Fig. 3A, there are ~ 500 electrons added to the extra dot as V_g is swept from 0 to 9 V. Remarkably, the period of the CB oscillations is not changing with the number of electrons in the dot. In Fig. 3B we plot the spacing between neighboring peaks as a function of V_g (or, equivalently, the number of electrons in the dot). As the number of electrons in the dot increases, the Fermi energy in the dot rises and the area of the dot changes, following the shape of the confining potential, as shown schematically in Fig. 3C. In order for the peak spacing and, thus, the gate capacitance, to be independent of the number of electrons in the dot, the confining potential should be very sharp. As an estimate, we use a mean level spacing of 1 meV, measured for the main dot. In this case, the Fermi energy for a dot with 500 electrons is 0.5 eV and only oxide can provide the required rigidity of the confining potential.

There is still an ambiguity to the extent where in the oxide the extra dot is formed. For example, we can imagine that the buried oxide is not completely removed from under the bridge and that the extra dot is

formed somewhere inside the buried oxide. We tested this conjecture experimentally by using Si substrate as a back gate (see the schematic in Fig. 1C). The back gate action on a MOSFET channel (without any e-beam lithography) is shown in Fig. 4A. Application of the back gate voltage V_{bg} shifts the threshold voltage of the device roughly in accordance with the back gate-to-front gate capacitance ratio of 1 : 18. In contrast, there is no V_{bg} dependence of peak positions for either the main or the extra dots, Fig. 4B. This result can be understood only if we assume that both the main and the extra dots are screened from the back gate by the poly-Si front gate. Thus, we conclude that the extra dot is formed within the gate oxide, which surrounds the main dot.

The conclusion that the extra dot is formed inside the gate oxide is consistent with all our observations and allows us to explain some previously published data on a similar footing. For example, CB in highly doped wires [10] is naturally explained by a conduction through the wire with some constriction, which is by-passed by a CB through the dot in the oxide. The data from both short-channel MOSFETs [9] and point contacts [8] can be simply understood as CB oscillations through a dot in the oxide superimposed on a regular MOSFET characteristics.

Unfortunately, at this point we are still lacking a good understanding regarding the origin of the extra dots. We can speculate that these dots are Si voids in the oxide, formed during oxidation. Possibilities for such a void formation could be different oxidation speeds for different crystallographic directions of the Si bridge, as well as intrinsic stresses within the oxide. The fact that similar dots are formed in samples from SIMOX and UNIBOND wafers [8] suggests that non-uniform oxidation is not the result of the damage from oxygen implantation in the SIMOX wafer.

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