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# Si/SiGe Nanostructures Fabricated by Atomic Force Microscopy Oxidation

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## ABSTRACT

In this work, local AFM oxidation technique in a controlled humidity environment has been used to create small features in strained SiGe alloys. When directly oxidizing SiGe alloys, minimum line widths of 20nm were achieved by adjusting parameters such as the bias voltage on the microscope tip and the tip writing speed. It was found that when bias voltage increases, and/or when the tip writing speed decreases, the oxidation height of silicon-germanium increases. In contrast to conventional thermal oxidation, the oxide height on SiGe alloys is slightly less than that on Si. Finally, this method was used to successfully cut conducting SiGe quantum well lines with high resolution.

## INTRODUCTION

Si/SiGe nanostructures are of great interest for future Si-based nanodevices, such as quantum dot transistors. Conventional fabrication techniques, such as electron beam lithography and reactive ion etching (RIE), are high-energy processes which can cause radiation and etching damage, leading to the possibility of interface states in quantum devices. Thus a low energy nanolithography process is an important technological challenge for the fabrication of nanostructure devices. Recently, atomic force microscopy (AFM) with low tip voltages (~20 V) under a controlled humidity environment has been used to locally oxidize silicon on a scale of 10's of nanometer [1]. Nanoelectronic devices using AFM oxidation have been fabricated on silicon, metal and gallium arsenide [2-4]. When oxidizing silicon, the nano-scale pattern of the oxide can be transferred into silicon substrate using the generated oxide as a mask [5]. However, AFM oxidation patterning of Si/SiGe heterostructures has never been demonstrated to the best of our knowledge, though strained Si/SiGe heterostructures give superior carrier transport mobility compared with silicon [6].

In this work, we reported the AFM oxidation of strained SiGe layers grown on a silicon substrate. Varying oxidation conditions, such as bias voltage and writing speed, height and width of SiGe oxide were studied. The AFM oxidation of SiGe was compared with that of silicon. Finally, the method was used to pattern the electrical conducting small SiGe wires.

AFM oxidation was performed at room temperature in tapping mode on a Digital Instruments Nanoscope III. While scanning tunneling microscopy (STM) offers the possibility of fine-features and AFM in contact mode has the advantage of a high writing speed, a trade-off between them is achieved in AFM tapping mode [7]. A heavily-doped silicon tip with curvature radius smaller than 10 nm was used (MikroMasch Inc.). In tapping mode, the AFM cantilever is driven by a piezoelectrode to oscillate at or near the resonant frequency (~ 300 kHz) of the tip cantilever. Before oxidation, the sample was first submerged in acetone for 10 min in an ultrasonic bath, and then dipped into a 10% diluted aqueous HF solution for 1 min. A subsequent deionized water rinse for 1 min led to Si or SiGe surface being passivated with a hydrogen. During AFM writing, a feedback loop kept the tapping amplitude (and thus the average distance

from sample surface to the tip) constant. The relative humidity kept constant at ~ 70% by bubbling nitrogen through water into an environment chamber surrounding the tip. The bias voltage on the tip with respect to the sample was varied from –10V to –40 V. The tip movement was controlled by software to form the oxide pattern we wanted. Three kinds of samples were used in our experiment: boron doped p-type silicon wafer with the resistivity of 10 Ω·cm, strained $Si_{0.8}Ge_{0.2}$ layer with a thickness of ~ 10 nm deposited on a silicon (100) substrate by rapid thermal chemical vapor deposition (RTCVD), and finally a p-doped $Si_{0.7}Ge_{0.3}$ layer on silicon capped with a thin (~ 2 nm) Si layer.

## AFM OXIDATION OF SILICON-GERMANIUM ALLOYS

In AFM oxidation, the electric field from the tip causes the dissociation of water, leading to anodic oxidation of the substrate. Because the oxide has about twice volume of the silicon or silicon-germanium consumed, the oxidation region has a height higher than that of the rest of the surface. Fig. 1 shows a set of oxidation lines of strained $Si_{0.2}Ge_{0.8}$ by AFM lithography with the tip bias voltage of -12V and tip writing speed of 1.0 μm/s. The full width at half magnitude (FWHM) of the oxidized lines is smaller than 20 nm. AFM oxidation on strained $Si_{0.2}Ge_{0.8}$ at different bias voltages before and after the removal of oxide by HF selective etching is shown in Fig. 2(a) and Fig. 2(b) respectively. The bias voltage applied on the tip during local oxidation was varied from –10 V to –32 V, corresponding to each line shown in Fig. 2(a). The oxide lines are faithfully transferred into the SiGe alloy by the HF etching (Fig. 2(b)). Fig. 2(c) shows the topography profile along the arrow lines indicated in (a) and (b). The ratio of peak heights of the oxide lines after oxidation to the valley depths after oxide removal is about 3: 2. This corresponds to a ratio of SiGe removed to the total oxide thickness of ~ 0.4. This is close to that observed in conventional silicon oxidation of ~ 0.44. The oxide height, depth and width as a function of bias voltages are plotted in Fig. 3. It is very evident that the height, depth and width of the oxide all increase approximately linearly with the bias voltage. Oxidation lines with FWHM less than 20 nm are obtained at a bias voltage smaller than –14 V.

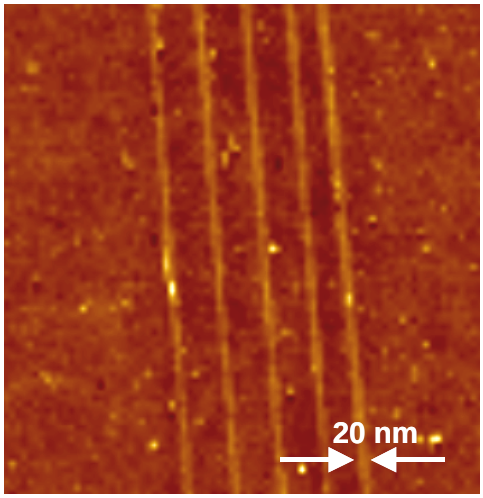


**Figure 1.** Fine oxide lines on strained $Si_{0.8}Ge_{0.2}$ by AFM lithography at the bias voltage –12V.

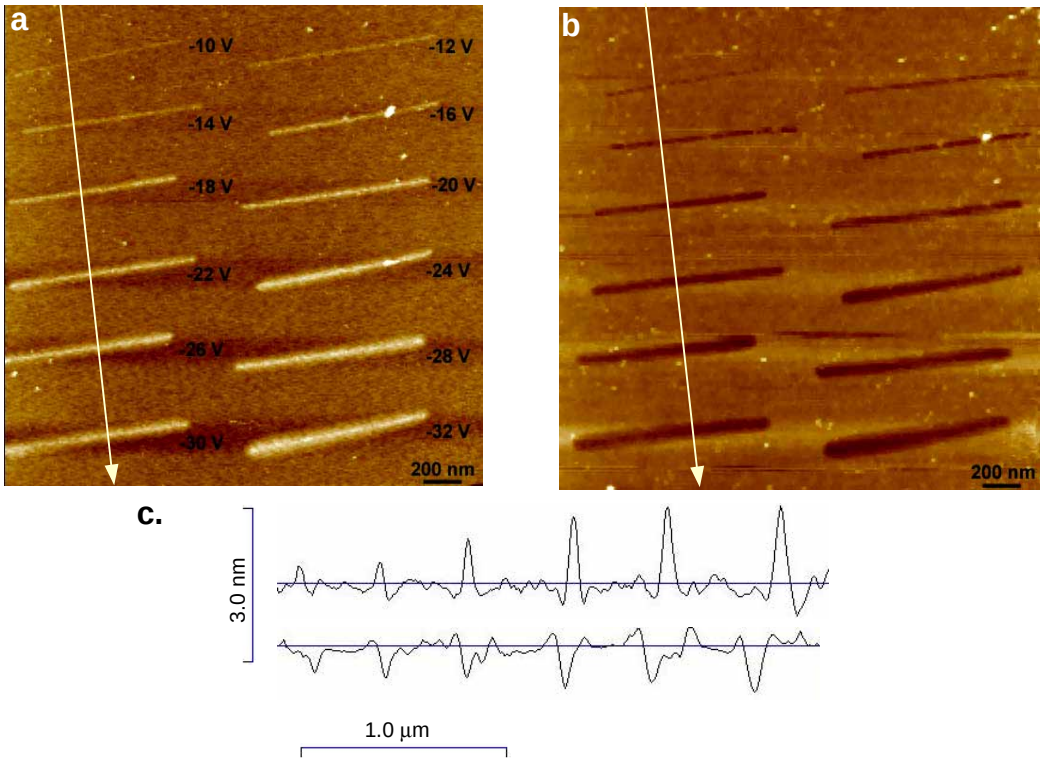


**Figure 2.** AFM oxidation lines of $Si_{0.8}Ge_{0.2}$ with different bias voltages between the tip and sample. The scan speed was 1.6 µm/s, and tapping amplitude setpoint was 0.04 V. (a) after oxidation; (b) after removing oxide by HF; (c) height profile along arrow lines in (a) and (b).

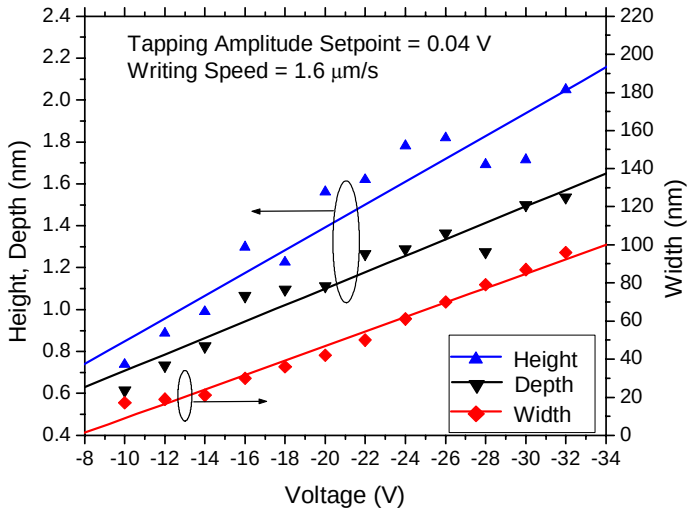


**Figure 3.** Feature height, depth (after HF etching) and FWHM as a function of the bias voltage for AFM oxidation of $Si_{0.8}Ge_{0.2}$.

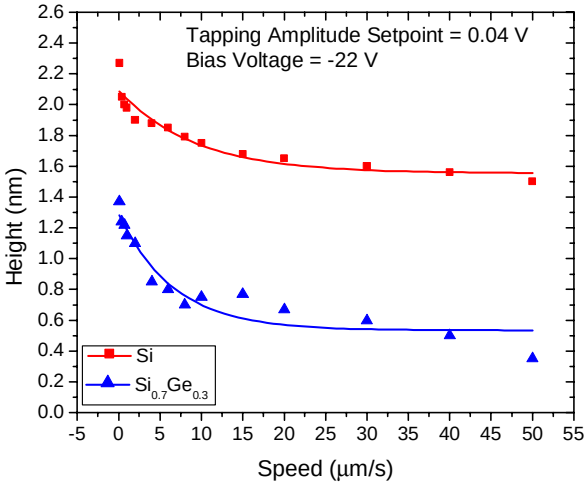


**Figure 4.** Oxide height of AFM oxidation on silicon and $Si_{0.7}Ge_{0.3}$ as a function of writing speed.

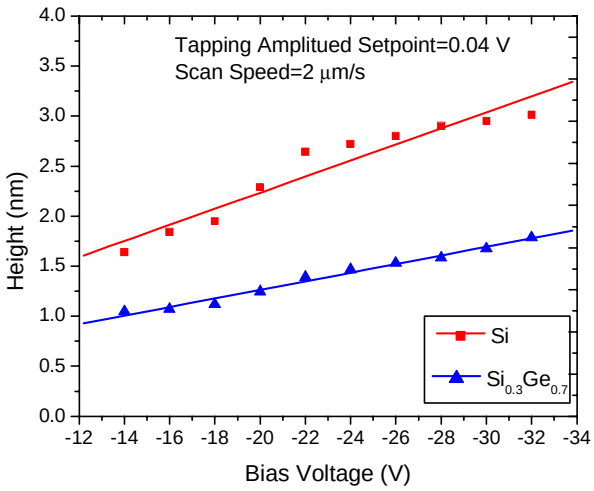


**Figure 5.** Comparison of feature height from AFM oxidation of Si and $Si_{0.7}Ge_{0.3}$ as a function of the bias voltage.

Snow and Campbell [1] have proposed field-assisted anodic oxidation as the mechanism of AFM oxidation of silicon. The electric field resulting from the voltage between the tip and the sample generates hydroxyl ions from the water vapor, and $OH^-$ ions react with holes ($h^+$) from the Si surface to form silicon dioxide: $Si + 2h^+ + 2OH^- \rightarrow SiO_2 + 2H^+$. We assume a similar model describes the oxidation of silicon-germanium. The oxidation rate is limited by the formation of $OH^-$, which explains our observations of the increase of oxide height as the bias voltage increases.

The oxidation rate is almost constant for scan speeds above 20 μm/s (Fig. 4), and increases markedly for slower speeds. At a speed of 2 μm/s with a tip voltage of –22V, the oxide height formed on $Si_{0.7}Ge_{0.3}$ is ~ 1.6 nm, corresponding to an oxide thickness ~ 2.4 nm. Under this condition, the linewidth is ~ 60 nm. To reduce the linewidth to 20 nm, the voltage must be lowered to ~ 14V, and the oxide thickness is only ~ 1.8 nm. Thus for high-resolution patterning, the amount of oxide grown (or SiGe consumed) is small.

In Fig. 4 and Fig. 5, the oxidation of $Si_{0.7}Ge_{0.3}$ and Si surfaces are compared. On both silicon and silicon-germanium, the oxide thickness decreases logarithmically with the increase of writing speeds and increases linearly with the increase of bias voltages. However, the feature height (and thus the oxide thickness) on $Si_{0.7}Ge_{0.3}$ is lower than on silicon. In contrast, under thermal wet oxidation (~ 800 °C), the oxides grown on SiGe can be 2.5 times thicker than those grown on silicon [8]. Thus the lower rate of AFM oxidation on silicon-germanium might be associated with a lower rate of water dissociation, rather than a lower rate reaction of the oxidizing species with SiGe, or with differences in the water adsorption on the sample surfaces. It has been reported that unlike on silicon, water does not stick easily on Ge(100) surface at room temperature [9]. Disappearance of infrared Ge-H stretching vibration when Ge(100) exposes to water at room temperature leads to a conclusion that either absorption does not occur (low sticking coefficient) or adsorption occurs without dissociation, which is in contrast with Si(100) with higher possibility of water dissociation [10]. However, how this relates to a $Si_{0.7}Ge_{0.3}$

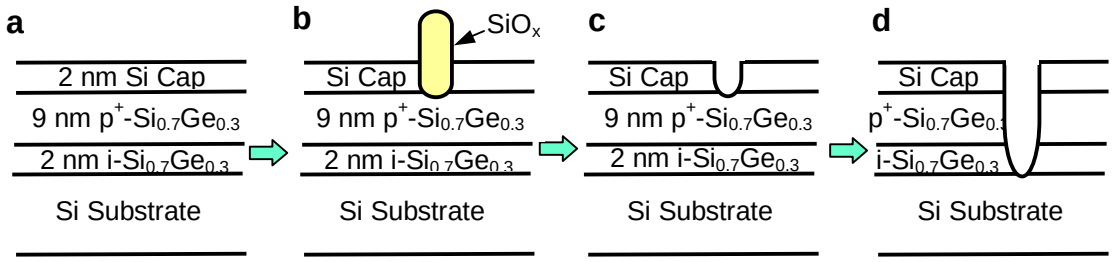


**Figure 6.** Process to pattern Si/SiGe nanostructure: (a) Layer structure; (b) Si cap AFM oxidation; (c) HF dip to remove $SiO_x$; (d) wet selective etching to pattern SiGe layer.

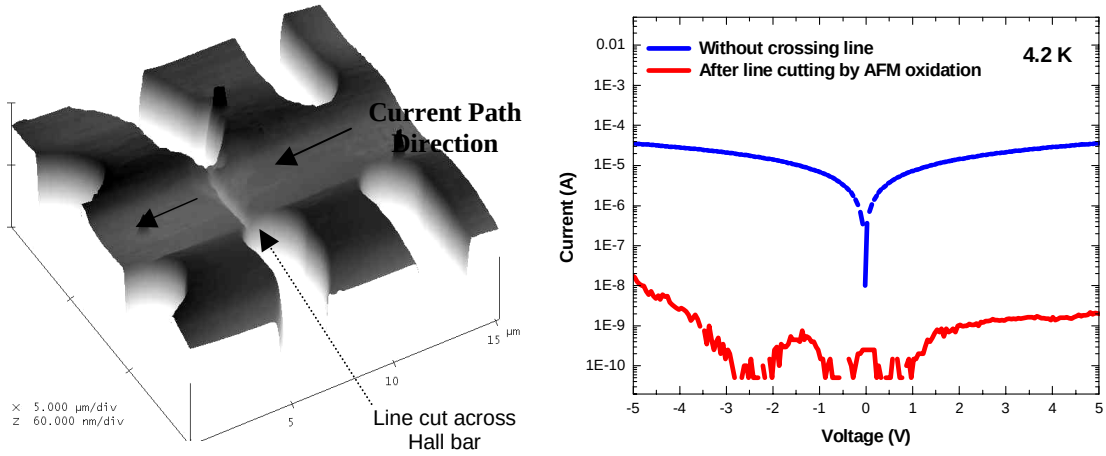


**Figure 7.** (a) AFM image of a line cut across Hall bar by AFM oxidation and selective wet etching in a sample with the layer structure of Fig. 6. The sample was pre-patterned by optical lithography and RIE to create mesa Hall bar structure. (b) Hall bar resistance measurement at T= 4.2 K before and after cutting the Hall bar by AFM oxidation and wet etching.

surface, and to the oxide surface which is present once oxidation begins, is not known. It should also be noted that we do not know at present if the oxide that forms has the same ratio of Si to Ge as in the substrate, or if the oxide is $SiO_2$ with Ge "snowplowing" ahead in front of oxide. Both cases have been observed during thermal oxidation under different conditions [11].

## ELECTRICAL STRUCTURES PATTERED BY AFM OXIDATION

Our long-term goal is to use AFM oxidation to pattern nanodevices in silicon-based heterostructures, such as Si/SiGe. From above experiments, the maximum thickness of SiGe oxidized by AFM lithography is ~ 3.0 nm, which is thinner than the layer thickness of SiGe in many nanostructure devices. Thus it is difficult to directly pattern a SiGe layer. Therefore, the layer structure shown in Fig. 6(a) was used with a modified pattern transfer approach. A 9nm-thick $p^+$-$Si_{0.7}Ge_{0.3}$ strained layer was first grown on silicon as a conduction layer, followed by a thin (~ 2 nm) Si cap. The holes are confined to the doped SiGe layer by the valence band offset.

The SiGe layer must be cut to laterally confine the holes to define small structures. First, the 2nm-thick silicon cap layer was locally oxidized by AFM (Fig. 6(b)), the silicon oxide was subsequently removed by diluted HF (Fig. 6(c)), and finally selective wet etching (HF: $H_2O_2$: $CH_3COOH$ = 1: 2: 3) of the SiGe transferred the pattern into the strained $Si_{0.7}Ge_{0.3}$ layer (Fig. 6(d)).

For electrical measurements, a Hall bar was fabricated by first etching Si and SiGe by optical lithography and RIE. This created a mesa structure with a height of ~ 200 nm. Aluminum contacts were also made. A line was cut through the current path in the SiGe layer Hall bar (Fig. 7(a)) by AFM oxidation of silicon and wet etching as described above. The I-V characteristics of the device were measured at 4.2 K (Fig. 7(b)). The resistance of Hall bar increases from ~ 100 kΩ before the line was cut to ~ 3.0 GΩ after the SiGe layer was cut, clearly indicating the complete separation of the $p^+$-SiGe quantum wells. (The measurement we performed at low temperature was to prevent holes from thermally escaping into the silicon substrate, which would have provided a shunt conductance path across the region of the missing SiGe.)

## CONCLUSIONS

AFM has been successfully used to pattern strained SiGe films by local oxidation, and lines with FWHM smaller than 20 nm were demonstrated. The height of the generated oxide increases with the increase of bias voltage between the tip and the sample and/or with the decrease of the tip writing speed. The oxide thickness of SiGe grown by this method is lower than that grown on Si. Si/SiGe nanolines have been fabricated by this AFM oxidation and selective wet etching and demonstrated electrically.

## ACKNOWLEDGEMENT

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