Nanopatterning of Si/SiGe electrical devices by atomic force microscopy oxidation

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Two nanopatterning methods for silicon/silicon-germanium (Si/SiGe) heterostructures are demonstrated: (1) direct atomic force microscopy (AFM) oxidation on SiGe layers and (2) AFM oxidation on silicon followed by selective wet etching of SiGe. When directly oxidizing SiGe alloys, minimum linewidths of 20 nm were achieved by adjusting the bias voltage of the AFM tip. By AFM oxidation and selective wet etching, a 10-nm-thick conducting SiGe layer was patterned to form features under ~50 nm. Fabricated SiGe quantum dots with side gates exhibited Coulomb blockade oscillation. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1515113]

Si/SiGe heterostructures have much higher carrier mobility than silicon field-effect transistors.[1,2] Si/SiGe nanodevices, such as quantum dots, may offer new device functionality. Therefore, nanopatterning of Si/SiGe heterostructures has been of great interest. The conventional nanofabrication techniques are electron-beam lithography and reactive-ion etching (RIE). These are high-energy processes which can cause radiation and etching damage, leading to the possibility of interface states or deep levels in quantum devices. Thus, a low-energy patterning process is an important technological challenge for the fabrication of nanostructure devices. Recently, atomic force microscopy (AFM) with low tip voltages (~10 V) under a controlled humidity environment has been used to locally oxidize silicon. The oxide feature size is on a scale of tens of nanometers.[3] Nanoelectronic devices using AFM oxidation have been fabricated on silicon, metal and gallium arsenide.[4–6] However, AFM oxidation patterning of Si/SiGe heterostructures has never been demonstrated to the best of our knowledge, although strained Si/SiGe heterostructures give superior carrier transport mobility compared with silicon. In this work, AFM methods of nanopatterning Si/SiGe heterostructures are demonstrated. AFM local oxidation on a strained SiGe layer grown on a silicon substrate was tested. Finally, a SiGe quantum dot was fabricated by AFM oxidation and wet etching.

AFM oxidation was performed at room temperature in tapping mode on a Digital Instruments Nanoscope III. A silicon tip with nominal curvature radius smaller than 10 nm was used. During AFM writing, a feedback loop was enabled. Compensation for the change of tapping amplitude due to bias voltage[7] was not made. The relative humidity was kept at ~70% by bubbling nitrogen through water into an environment chamber surrounding the tip. Two kinds of samples were used in our experiment: a pseudomorphic 10-nm-thick strained $Si_{0.8}Ge_{0.2}$ layer deposited on a silicon (100) substrate by rapid thermal chemical vapor deposition, and a heavily *p*-doped pseudomorphic 10-nm-thick $Si_{0.7}Ge_{0.3}$ layer on silicon capped with a thin Si layer with thickness of ~2 nm.

The first nanopatterning method used was direct AFM oxidation of the SiGe layer. Isolated line scans were performed with a tip bias voltage between −10 and −32 V with respect to the substrate. During AFM lithography, the tip writing speed was ~1.6 μm/s. The resulting volume expansion associated with oxidation causes a raised oxide feature to appear, which was characterized in a regular AFM scan. HF wet etching to remove the oxide faithfully transferred the feature into the SiGe alloy. A minimum linewidth [full width at half magnitude (FWHM)] of less than 20 nm occurs with a bias voltage −14 V, causing a feature ~1.0 nm above the surface after oxidation and a depression of ~0.8 nm after oxide removal. The oxide height, depth and width all increase with the bias voltage (Fig. 1). The ratio of peak heights of the oxide lines after oxidation to the valley depths after oxide removal is about 3:2. This corresponds to a ratio of SiGe removed to the total oxide thickness of ~0.4, which is close to that observed in conventional silicon oxidation of ~0.44.

Snow and Campbell[3] have proposed field-assisted anodic

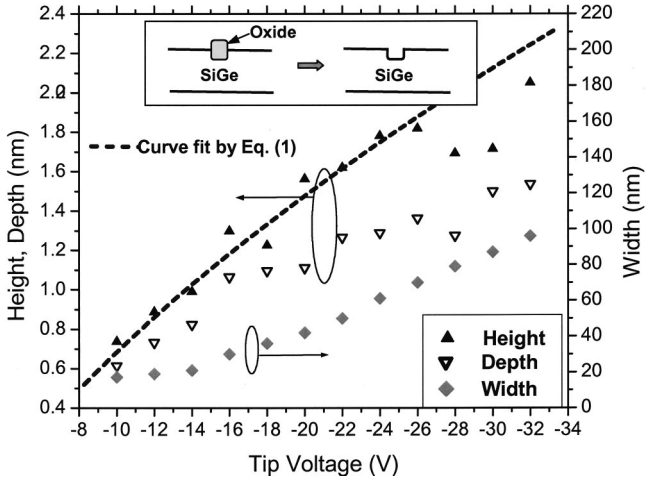

FIG. 1. Height, depth (after HF etching) and FWHM of AFM oxidation lines on strained $Si_{0.8}Ge_{0.2}$ alloys as a function of different bias voltages between the tip and sample. The writing speed was 1.6 μm/s. The dashed line is a fit of the height data using Eq. (1). The inset is a schematic of AFM oxidation and oxide removal.

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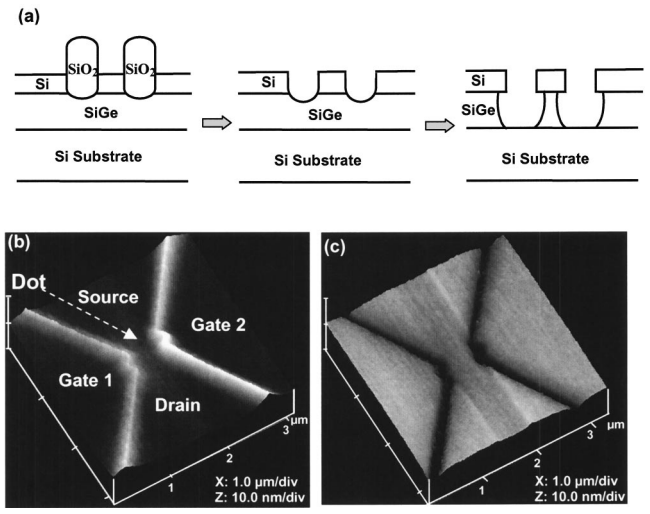

FIG. 2. (a) Process to pattern Si/SiGe nanostructures: AFM oxidation on the Si cap; HF dip to remove SiO_2; and wet selective etching to pattern the SiGe layer. (b), (c) AFM images of a SiGe quantum dot fabricated by this nanopatterning approach after AFM oxidation and selective wet etching, respectively.

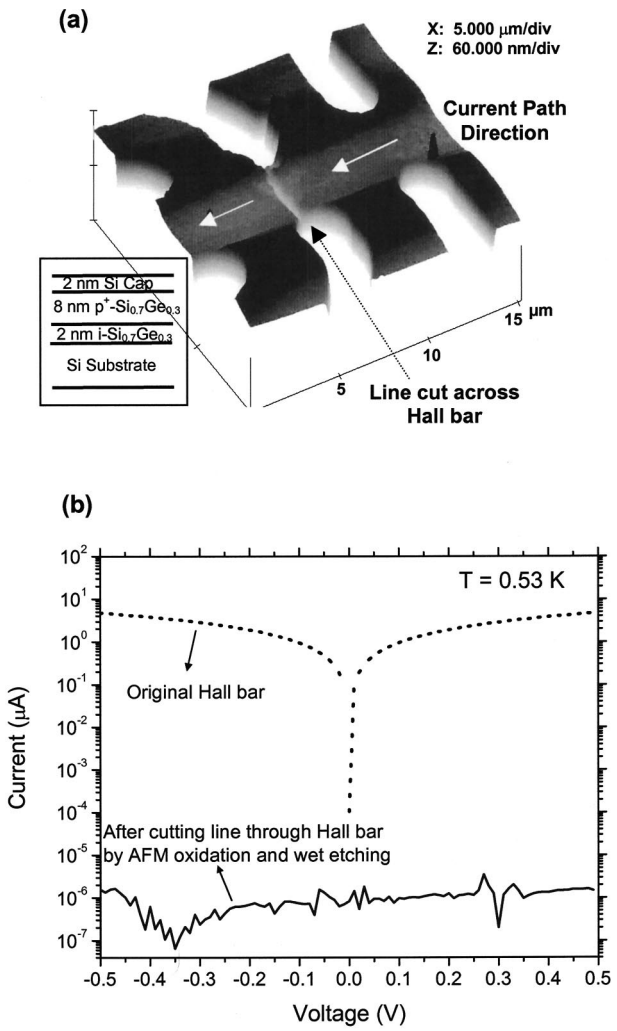

FIG. 3. (a) AFM image of a line cut across the Hall bar by AFM oxidation and selective wet etching. The sample was pre-patterned by optical lithography and RIE to create a mesa with Hall bar structure. (b) Hall bar resistance measurement at $T=0.53$ K before and after cutting a line across the Hall bar.

oxidation as the mechanism for AFM oxidation of silicon. This involves three steps: (1) water vapor adsorbs on the silicon surface; (2) the electric field resulting from the voltage between the tip and the sample dissociates water into hydrogen (H^+) and hydroxyl (OH^-) ions; (3) OH^- ions react with holes (h^+) from the Si surface and form silicon dioxide. The chemical reaction is $Si+2h^++2OH^-\rightarrow SiO_2+2H^+$. We assume a similar model to describe the oxidation of SiGe. That the oxidation rate depends on the tip voltage (and thus electric field) suggests that the rate is limited by the formation of OH^-. The step height h was fitted to the following model, which was used to describe the kinetics of AFM oxidation:[8]

$$h(t,V)=V/E_0\ln[RE_0t/V+1], \tag{1}$$

where V is the tip bias voltage, t is the exposure time to the electrical field, and R and E_0 are constants. The best fit was given by $E_0=45$ V/nm (the same as for Si in Ref. 8) and $R=1050$ nm/s.[9] For similar conditions in our approaches, we found AFM oxidation of silicon gives an oxidation feature ~50% higher than that which occurs on SiGe.[10] Thermal oxidation typically gives a thicker oxide on SiGe than on Si,[11] indicating a different mechanism of oxidation in this AFM case.

From the above experiment, one finds that the maximum thickness of SiGe oxidized by AFM lithography is ~2.0 nm. This is thinner than the layer thickness of SiGe in many nanostructure devices, so devices with a SiGe layer thickness greater than 2.0 nm cannot be completely patterned by a single direct AFM oxidation step. Therefore, the layer structure shown in Fig. 2(a) was developed. First, the 2-nm-thick silicon cap layer was locally oxidized by AFM; then the silicon oxide was subsequently removed by diluted HF; and finally, wet etching ($HF:H_2O_2:CH_3COOH=1:2:3$) of the SiGe with a selectivity ~400:1 over silicon[12] transferred the oxide pattern into the strained $Si_{0.7}Ge_{0.3}$ layer [Fig. 2(c)]. A demonstration of this nanopatterning technique is shown in Figs. 2(b) and 2(c). Compared with direct AFM oxidation, this second method reduces pattern resolution due to anisotropy of the wet etching, and increases the minimum linewidth from 20 to 50 nm. However, 10-nm-thick SiGe layers were successfully patterned by this approach.

Using AFM oxidation and selective wet etching, several Si/SiGe electrical nanodevices were fabricated. First, we demonstrate that a narrow gap could be cut through a p^+-$Si_{0.7}Ge_{0.3}$ strained layer of thickness ~10 nm [shown in Fig. 3(a)]. At low temperatures, holes are confined to the doped SiGe layer by the valence band offset, so that cutting a line through the SiGe layer should break the electrical conduction of that layer. A Hall bar ~4 μm wide was first patterned by optical lithography and RIE, creating a mesa with height of ~200 nm. A line was subsequently cut through the current path in the SiGe layer Hall bar [Fig. 3(a)] by AFM oxidation and selective wet etching as described above. The $I-V$ characteristics of the device were measured at 0.53 K [Fig. 3(b)]. The resistance of the Hall bar increases from ~10 MΩ before the line was cut to ~10^7 MΩ after the SiGe layer was cut, clearly indicating complete cutting of the p^+-SiGe layer. (The measurement was performed at low temperature to prevent holes from thermally escaping into

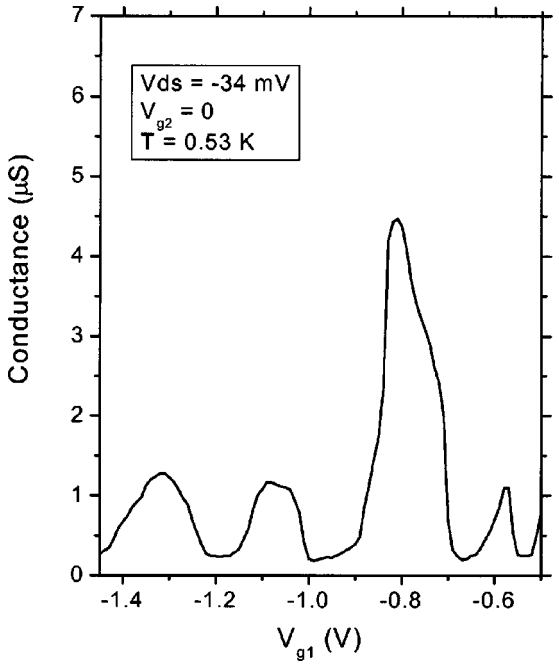

FIG. 4. Electrical characteristics (conductance vs gate voltage) of a SiGe quantum dot fabricated by AFM oxidation and selective wet etching that exhibits Coulomb blockade oscillation at $V_{ds}=-34$ mV and $T=0.53$ K.

the silicon substrate, which would have created a shunt conductance path across the region of the missing SiGe.)

A SiGe quantum dot was also fabricated with the same Si/p^+-SiGe/Si layer structure. Figure 2(b) shows the dot structure after AFM oxidation. The size of the SiGe dot after wet etching is expected to be smaller than 100 nm. The lateral confinement in the narrow regions adjacent to the source/drain forms potential barriers on both sides of the dot. The two coplanar SiGe regions on either side of the dot are electrically insulated from it (by cutting the SiGe layer), and thus serve as lateral gates, which can modulate the electrical potential in the dot. Similar structures have been made in doped SiGe layers on silicon-on-insulator substrates by electron-beam lithography and RIE.[13] At low temperatures, the source–drain current exhibits oscillations as a function of the gate voltage, and is associated with Coulomb blockade. An example of such data is shown in Fig. 4 for $T=0.53$ K. In this device the oscillations are not perfectly periodic, the current has considerable noise, and V_g scans in different directions are not reproducible. We attribute these effects to the large number of traps on the surface of the SiGe. In the dot, the electron wave function extends to the surface of the etched region, which is not passivated (except by a thin native oxide). Thus, trapping/detrapping of charges at the surface are expected. Currently, we are working to improve the surface passivation to eliminate charge traps at the dot–insulator interface. Nevertheless, the results clearly show the use of AFM local oxidation and wet etching as a low-energy patterning technique for Si/SiGe nanodevices.

In summary, AFM was used to pattern strained SiGe films by local oxidation, and lines with FWHM smaller than 20 nm were demonstrated. The maximum amount of SiGe consumed is ~1.5 nm, which is ~50% less than that of Si. AFM oxidation of silicon plus selective wet etching was used to pattern thicker SiGe layers and to fabricate Si/SiGe nanodevices. Electrical measurement of a SiGe quantum dot shows Coulomb blockade oscillation, demonstrating the capability of this nanopatterning technique.

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