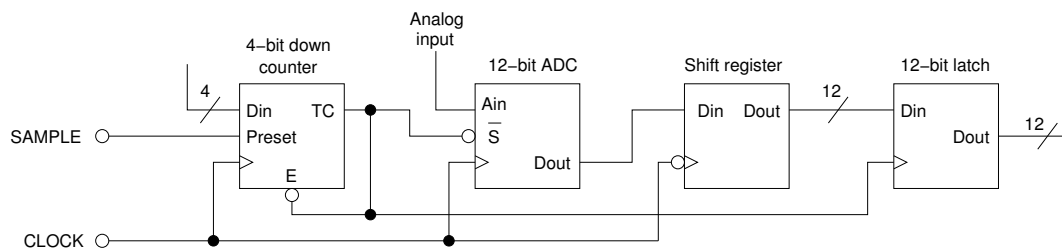


Physics 536 - Assignment #9

1. Show how a D flip-flop can be configured to divide the frequency of a clock signal by two. Draw a timing diagram for the clock input, and the Q and $\overline{Q}$ outputs.

2. A computer with a 16-bit address bus and an 8-bit data bus uses 8192x8 bit memory chips. If each memory chip has an active-low enable input, show how the full 16-bit address space can be implemented using 8 of these memory chips and an additional 3-bit to 8-line decoder with active-low outputs.

3. Consider the following circuit:



The components shown in the diagram perform the following functions:

- **4-bit down counter:** When PRESET is high, the counter is set to the 4-bits of input data. In this case these are set to a constant value that you will need to determine. When the enable input is low, a rising edge of the clock input causes it to count down by one. When it reaches zero, the TC output will go high, indicating that the *terminal count* has been reached.
- **12-bit ADC:** On the falling edge of the S input, the analog input is sampled and a 12-bit digital representation of this value is shifted out on the DOUT output. Each rising edge of the clock input shifts out the next bit of the digitized output.
- **Shift register:** On each falling clock edge, the DIN input is shifted into the lowest bit of the 12-bit DOUT output.
- **12-bit latch:** On the rising edge of the clock input, the 12-bit input data, DIN is latched and driven to the output, DOUT.

Assuming that the clock signal has a 50% duty cycle, and that the SAMPLE input goes high briefly to initiate the conversion, draw the rest of the timing diagram for the PRESET, TC, the ADC DOUT, the shift register DOUT, and the latch DOUT. Select a value for the 4-bit DIN input to the down-counter that will give the correct 12-bit output that represents the analog input.