Design and Simulation of a Graphene DEPFET Detector

Ozhan Koybasi, Isaac Childres, Igor Jovanovic, Yong Chen

***Abstract*– Graphene field effect transistors (GFETs) fabricated on undoped semiconductor substrates have shown promise for sensing ionizing radiation with a potential of high sensitivity, low noise, low power, and room temperature operation. Radiation detection with GFET is based on the high sensitivity of graphene resistivity on local electric field perturbations caused by ionized charges generated in an electrically biased radiation absorbing semiconductor substrate. Those charges are drifted to the neighborhood of graphene by the gate voltage applied across the detector. GFET radiation sensors can be fabricated on a variety of substrates, exploiting their distinct material properties, to address different application regimes. The current simple GFETs lack the functionality of efficiently removing ionized charges accumulated underneath graphene after signal readout, which results in a slow response to irradiation cut-off and therefore compromises the ability to operate in the pulse mode. In order to overcome this limitation, we propose here a more advanced device architecture, namely, graphene DEPFET.**

I. Introduction

GRAPHENE, a single layer of carbon atoms tightly bound in a two-dimensional (2D) hexagonal crystal lattice, has attracted tremendous scientific and technological research interest in recent years with a great promise of being used as a next generation electronic material due to its exceptional properties [1]. Among many useful properties of graphene that have led to a very wide range of applications, we are particularly interested in the high sensitivity of its resistivity to local electric field variations [2] to implement graphene-based radiation sensors that potentially outperform the current semiconductor detector technologies in terms of higher sensitivity and resolution, and lower electronic noise, power consumption, and cost. In this scheme the detection of ionizing radiation is realized by applying a gate voltage across a graphene field effect transistor (GFET) fabricated on an undoped semiconductor substrate to alter the local electric field at graphene and consequently gives rise to a change in graphene conductivity. Different from the well-known semiconductor detectors, GFET features a novel detection concept that is based on sensing the electric field changes due to ionization in the substrate instead of collecting and measuring the amount of radiation-induced charge.

In this paper, after describing the device structure, operation principle, and measurement scheme of our GFETs, we provide a brief overview of the preliminary experimental results and discuss the main issues arising in our simple GFET devices. The remainder of the paper focuses on the design of a graphene DEPFET detector by utilizing TCAD simulations in order to address these issues. Graphene DEPFET sensors are expected to perform significantly better than simple GFETs in terms of response speed and sensitivity.

II. Device Structure, Operation Principle, And Measurement Scheme

The GFET device structure, detection concept and measurement schematics are depicted in Figure 1. Our prototype GFET sensor is made of a graphene layer on an electrically gated, nominally undoped radiation absorber substrate with an optional insulating layer in between. A gate voltage, V_G, is applied across the sensor to generate an electric field, which is varied to find the optimum point on the Dirac curve for a sharp change in graphene resistance. The passage of radiation through the radiation absorber increases the conductivity of the substrate via ionization, causing a higher potential drop across the dielectric under graphene and consequently a larger electric field in the vicinity of graphene at a fixed gate voltage. Figure 1c illustrates the electric field dependence of graphene resistance for exfoliated graphene on a doped silicon substrate. In order to obtain the greatest change in graphene resistance due to incident radiation, the device is operated at a gate voltage that leads to a local electric field corresponding to or around the Dirac peak in resistance before radiation exposure. Graphene resistance then exhibits a sharp drop under radiation due to increasing electric field. The operation of GFET as a radiation sensor, including its numerical modeling, is described in more detail in [3].

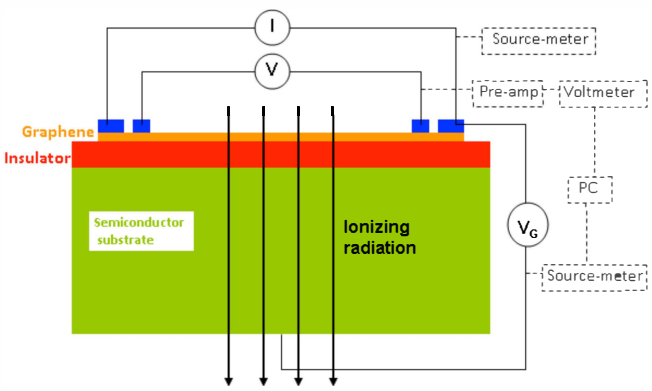
This work has been supported by Department of Homeland Security and Department of Defense under awards 2009-DN-077- AR1036- 02 and HDTRA 1-09-1-0047, respectively.

O. Koybasi was with Department of Physics and Birck Nanotechnology Center, Purdue University, West Lafayette, IN. He is now with Massachusetts General Hospital and Harvard Medical School, Boston, MA. (Phone: +1 617-724-3260, e-mail: okoybasi@partners.org)

I. Childres is with Department of Physics, Purdue University, West Lafayette, IN (e-mail: ichildre@purdue.edu)

Igor Jovanovic is with Department of Mechanical and Nuclear Engineering, Pennsylvania State University, University Park, PA. (e-mail; ijovanovic@psu.edu)

Y. P. Chen is with Department of Physics, Department of Electrical and Computer Engineering, and Birck Nanotechnology Center, Purdue University, West Lafayette, IN (e-mail: yongchen@purdue.edu)



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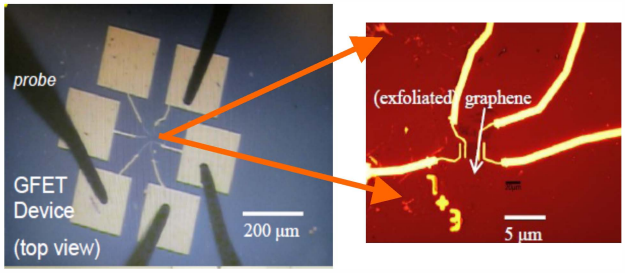

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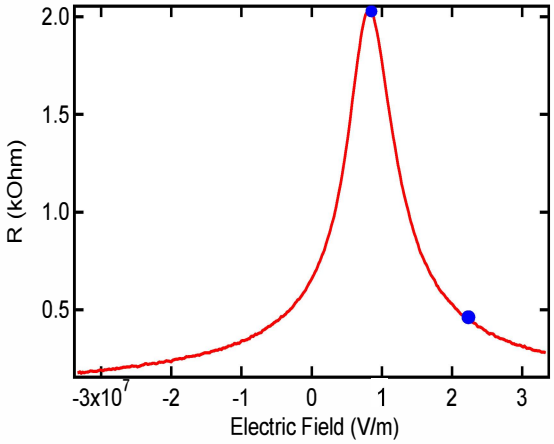

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Figure 1. a) GFET device structure and experimental schematics for radiation detection b) A representative GFET device picture. c) Graphene exhibits a sharp peak ("Dirac point") in resistance as a function of the electric field. Data shown are measured in a representative GFET made of exfoliated graphene on a doped Si substrate with 300 nm-thick SiO_2 as buffer layer at room temperature.

Four electrodes are fabricated on graphene in order to allow accurate 4-probe measurement of graphene resistance by eliminating the contact resistance, although a 2-probe measurement could be used in many practical situations. The two outer electrodes are used to supply the current through the graphene, while the inner two electrodes are used to measure the voltage drop across the graphene. Resistance measurements are performed using a lock-in amplifier for the experimental data presented in this paper.

III. Experimental Background

In order to fabricate GFETs that are optimal for a specific application regime, we can use different substrate materials, exploiting their most advantageous properties for the application regime under consideration: high bandgap for room temperature operation, low bandgap for better energy resolution, high carrier mobility for high response speed, large stopping power for detection of high energy photons, long carrier lifetime to minimize signal loss and enhance radiation hardness, and low cost for large scale manufacturing. The main benefit of using a Si substrate would be the low cost, while GFET made on SiC has the advantage of being operable at room temperatures and even above room temperatures due to its large bandgap of ~3.1 eV. On the other hand, CdTe substrate would be ideal for detecting high-energy photons with high efficiency due to its high density (~5.8 g/cm^3) and large atomic numbers of Cd (Z=48) and Te (Z=52), which give rise to a high stopping power [4]. Moreover, due to the large energy bandgap of CdTe (E_g=1.52 eV), detectors made of this crystal can also be operated at room temperature.

GFETs for radiation detection were first fabricated on Si absorber substrate and tested with X-ray photons. Measurements were performed using a small X-ray tube (Amptek) which can provide X-rays with energy and flux in ranges of 5-40 keV and 10-200 µA, respectively. Si absorber based GFETs did not show any response to radiation at room temperature due to the fact that a substantial amount of free charges still exist in undoped Si. The radiation sensor was irradiated with X-rays at cryogenic temperatures, and a clear response was observed at temperatures of 150 K and below. At a temperature of 4.3 K, the graphene resistance changed by more than 50% when the X-ray energy and flux was varied from (15 keV, 15 µA) to (40 keV, 80 µA) at a gate voltage of -20 V. Also as a proof of field effect concept, it was confirmed that there was no response to X-rays at zero gate voltage. Further details about X-ray response of Si absorber based GFET can be found in [5]-[6].

Some experimental results from GFETs fabricated on SiC using both epitaxial [7] and CVD [8] graphene growth techniques have also been reported [6], [9]. The SiC GFETs have a weak field effect but do not exhibit a Dirac peak. It has been demonstrated that the response is modified by X-rays, with graphene resistance decreasing at gate voltages of one polarity and increasing at gate voltages of the other polarity due to X-ray exposure, and the higher the X-ray energy or flux at a fixed gate voltage, the larger the change in graphene resistance. The relative change in graphene resistance due to (40 kV, 60 µA) X-ray irradiation has been measured to be as high as 70% at a gate voltage of -50 V at room temperature, which is promising. The reader is referred to [6] for further details on X-ray response of epitaxial graphene GFETs.

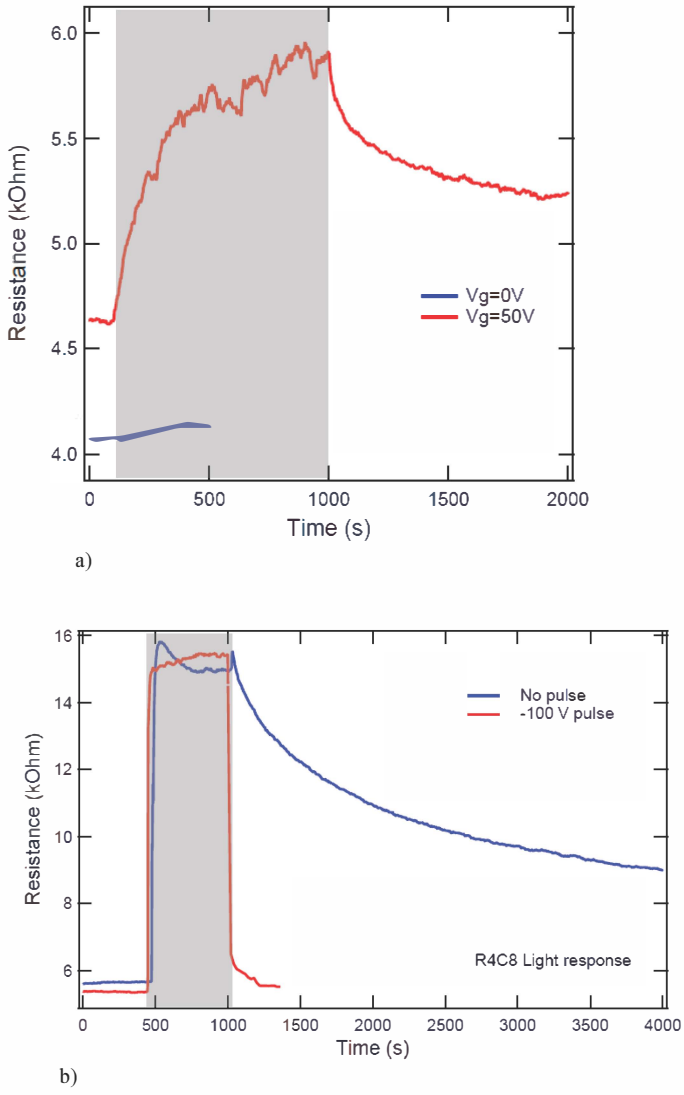


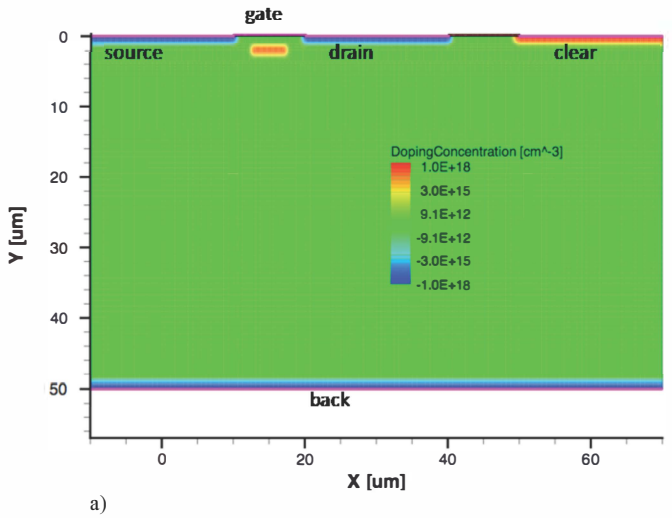
Figure 2. a) X-ray response and b) light response of CVD graphene FET on undoped SiC. Exposure intervals are shown in the gray. When turning off the light illumination is accompanied by a short voltage pulse with opposite sign to the gate voltage applied, resistance returns to its initial value much faster.

Figure 2 shows the X-ray and room ambient light response of CVD graphene FET on undoped SiC substrate at room temperature. Graphene resistance increases by about 200% when the device is exposed to light at a gate voltage of 50 V. A negligible response to X-rays was measured at zero gate bias, proving that the response of gated GFET is a field effect. This device suffers from a low response speed when the radiation source or light is turned off. In other words, graphene resistance is restored to its original value (before radiation exposure) over a relatively long period of time. This slow restoration of resistance is associated with the fact that our current devices lack a mechanism to effectively remove the ionized charges which are drifted to the top surface of the semiconductor substrate (due to the gate voltage applied across the absorber) and accumulated there. This has been experimentally confirmed by applying a short voltage pulse across the sensor thickness with opposite polarity to the gate voltage simultaneously with turning off the light. In this case, graphene resistance has been observed to return to its original value before any light exposure considerably faster, as shown in Figure 2 b. We are investigating more advanced device structures to address the draining of charges accumulated underneath graphene, which is the main focus of this paper.

IV. Graphene DEPFET

Our GFETs exhibit some similarities in the detection principle compared to the well-known DEPFET detectors [10]-[11], which have been extensively used in high energy physics and astrophysics for low noise and high resolution requirements, in the sense of providing simultaneous radiation detection and amplification functionality. Different from the DEPFET, however, our current simple GFET structure does not use a p-n junction to deplete the substrate to form a potential well to confine electrons near the transistor channel (graphene), and lacks a "clear" contact to drain the electrons from the potential well after readout. As discussed in the previous section, it can take a very long time (up to hours) for graphene resistance to return its pre-irradiation value after the radiation exposure ceases because of trapping of ionized charges at the semiconductor/insulator interface. Non-removal of these charges significantly degrades the sensitivity of the detector for the detection of next radiation event since the next event will just add charges to already existing considerable amount of charges at the interface. By implementing a graphene on DEPFET device architecture, we can accumulate the ionized charges in a potential well underneath graphene, and once the change in graphene conductivity due to the charges in the potential well is read out, we can clear the charges from the well by employing the clear mechanism available in the DEPFET architecture. As a result, this approach should be able to enable pulsed operation.

We have studied the structure and operation of DEPFET and optimized the device design with TCAD simulations to realize graphene DEPFET devices that will have the functionality we are missing in our current simple graphene FET devices. Figure 3.a shows the 2D silicon DEPFET structure and doping profile that we have simulated with Synopsys Sentaurus [12]. We define a mesh of discrete elements on this structure, and the simulation program solves the Poisson's equation along with carrier continuity equations at every grid point on the input mesh to calculate the electrical and physical quantities of interest. The mesh is more refined near the interfaces and regions of high doping gradient to improve the accuracy of the simulation. Carrier generation-recombination dynamics is modeled by Shockley-Read-Hall recombination. Different mobility models were employed to take into account doping dependent mobility degradation, mobility saturation at high fields and mobility degradation at interfaces.



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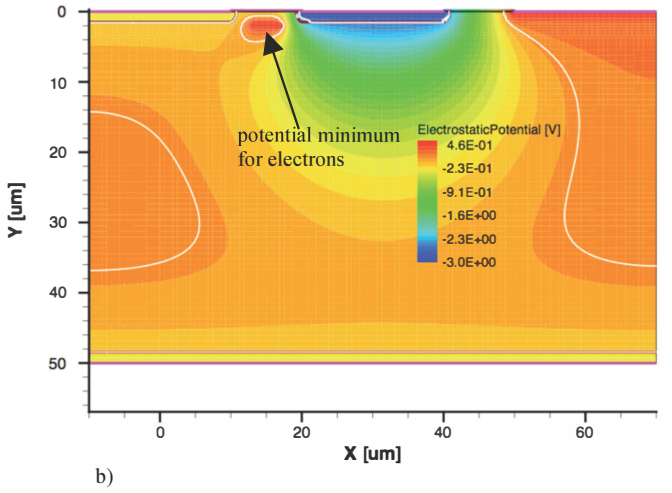

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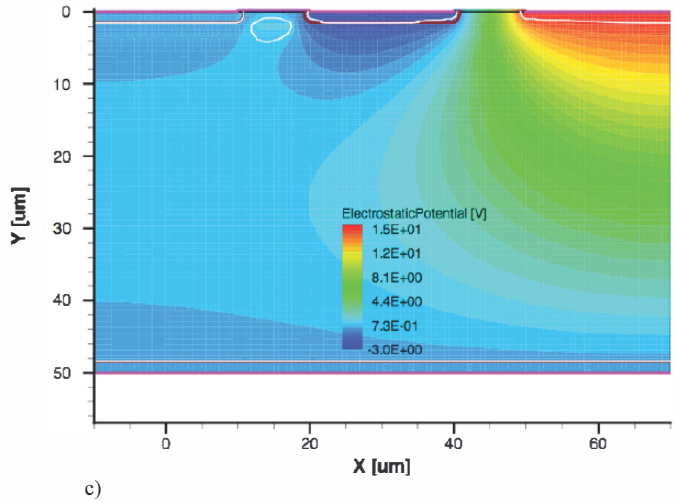

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Figure 3. a) Structure and doping profile of simulated DEPFET and corresponding electrostatic potential distribution in b) detection mode (V_{source}=0 V, V_{drain}=-2.5 V, V_{gate}=-1 V, V_{back}=0 V, V_{clear}=0 V) and c) clear mode ((V_{source}=0 V, V_{drain}=-2.5 V, V_{gate}=-1 V, V_{back}=0 V, V_{clear}=15 V). The white lines indicate the boundaries of the depleted region.

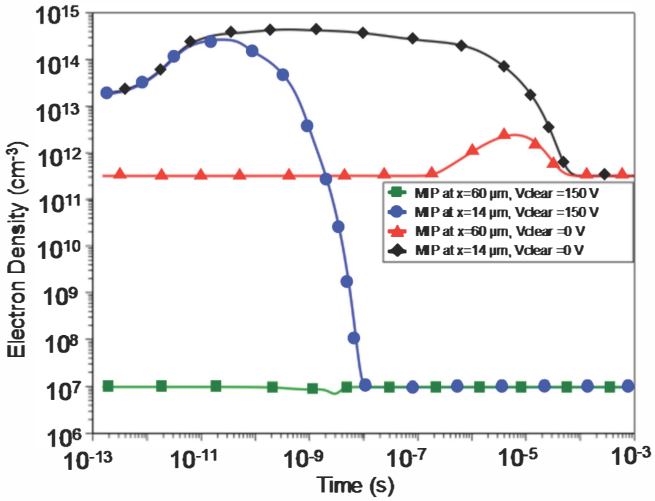

Figure 4. Simulated electron density in n-well vs. time due to MIP travelling across the detector at positions x=14 µm and x=60 µm for two different MIP positions both in detection and clear modes.

As displayed in Figure 3.a, an n-well is ion-implanted underneath the transistor channel for accumulating the radiation-induced electrons. The substrate is sidewards depleted by applying a negative voltage to the drain electrode while the source, back, and "clear" electrodes are grounded, as demonstrated in Figure 3 b. Radiation induced electrons can be confined in the n-well once it is fully depleted by applying a higher drain bias. After readout, the electrons are drained from this potential minimum by applying a positive voltage to the "clear" electrode. Figure 3 c shows the potential distribution when a positive voltage of 15 V is applied to the "clear" contact. In this case, all electrons migrate to the "clear" contact, which is the region of the lowest potential throughout the entire substrate.

Figure 4 shows the electron density in the n-well due to ionization generated by minimum ionizing particle (MIP) traversing the detector thickness vertically at two different positions: x=14 µm and x=60 µm. 80 electron-hole pairs per distance of 1 µm were induced along the MIP track, which is the most probable energy loss for MIP travelling through silicon. The lateral profile of the track is Gaussian with 1 µm standard deviation, so that ~99% of the charge is produced within a radius of 2.1 µm. Again, in order to improve the accuracy of the simulation, the mesh was refined along MIP tracks. Figure 4 indicates that electrons in the n-well are drained in approximately 5 orders of magnitude shorter time period when a positive voltage of 150 V is applied to the "clear" contact. Furthermore, simulated electron density in the n-well due to the passage of a minimum ionizing particle (MIP) at x=14 µm is $2x10^{14}cm^{-3}$, while it is only $2x10^{12}$ cm^{-3} when the MIP passes through x=60 µm, signifying that the majority of electrons generated on the right side of the detector are lost to the "clear" electrode. This is also evident in the potential distribution presented in Figure 3 b.

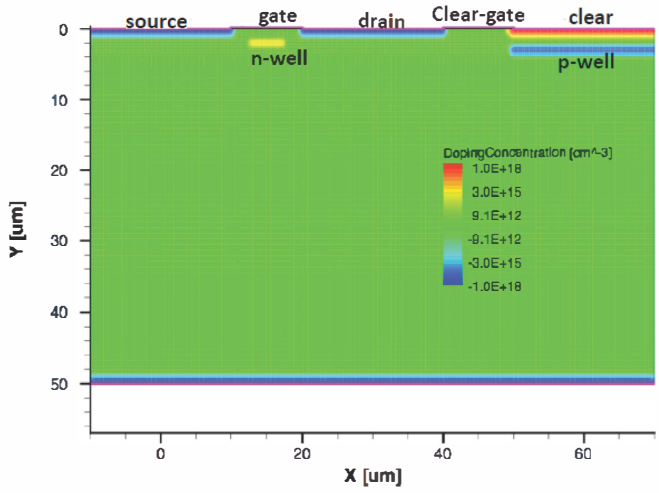

Figure 5. Improved DEPFET design with an additional p-well under the "Clear" electrode to prevent the charge loss to the "clear" contact in detection mode.

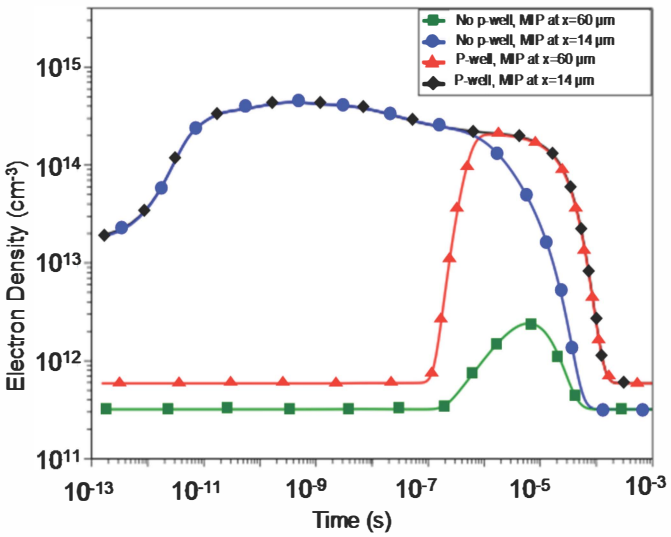

Figure 6. Simulated electron density in n-well vs. time due to MIP travelling across the detector at positions x=14 µm and x=60 µm with and without a p-well under the "clear" electrode.

The charge loss to "clear" electrode can be prevented by implanting a deep p-well under the "clear" contact (Figure 5), which reverses the direction of electric field under the "clear" contact, causing all electrons to drift to the n-well. This is illustrated in Figure 6. In the presence of a p-well under the "clear" electrode, the electron density in the n-well due to MIP ionization through x=60 µm is the same as the one due to MIP ionization through x=14 µm after charge drift to n-well is complete. Normally, it takes longer for carriers produced through x=60 µm to drift to the potential minimum since they have to travel a longer path. Figure 7 shows that the time it takes for ionized carriers to drift to the n-well when the MIP crosses the detector with the design featuring p-well under "clear" contact at different x-positions. Typically, the collection of charges in the n-well completes in the order 100 ns except for the MIP trajectory passing through the n-well.

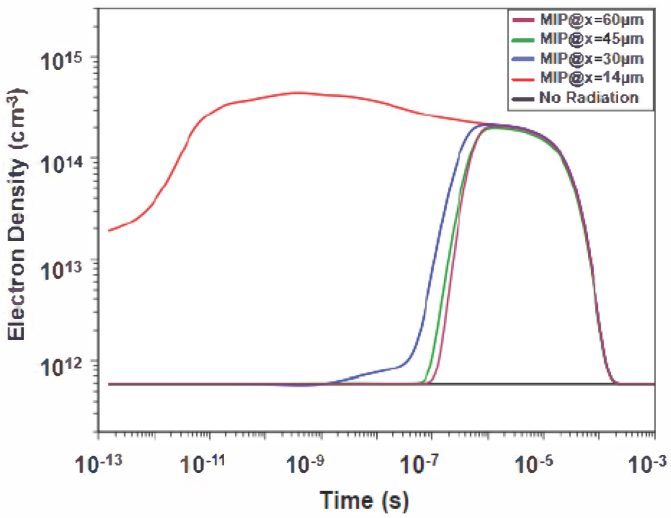

Figure 7. Carrier drift time for different MIP positions

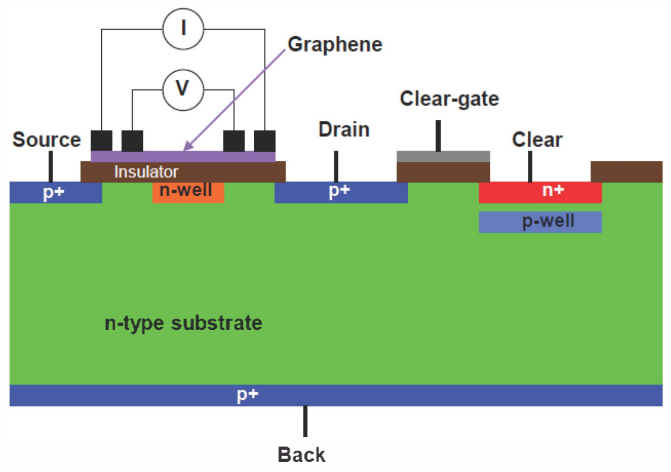

Figure 8. Graphene DEPFET device architecture optimized with TCAD simulations.

Existence of the p-well under the "clear" electrode produces a potential barrier which makes the process of clearing more difficult. A "clear-gate" electrode is introduced to control this potential barrier and the potential of the substrate neighboring the n-well [13]. 2D cross-sectional view of the graphene DEPFET structure we have designed with the aid of TCAD simulations is shown Figure 8. Instead of an inversion p-channel between source and drain, the transistor channel in our case is graphene deposited on the gate dielectric. In a normal DEPFET, the n-well is implanted a little below the p-channel so that electrons accumulated in the n-well can induce inversion p-channel at the semiconductor/ oxide interface. However, in case of graphene DEPFET, this inversion channel is not needed. The n-well is therefore implanted right at the semiconductor/oxide interface to confine charges as close as possible to graphene, which results in stronger modification of graphene resistivity.

V. CONCLUSION

We have demonstrated that gated GFETs fabricated on undoped semiconductor substrates can be used as radiation sensors featuring a novel detection concept with potentially improved capabilities. Our current efforts focus on developing a mechanism for confining radiation-induced charge carriers in the vicinity of graphene and draining them after readout by implementing a DEPFET architecture, which is essential to improve the response speed and sensitivity. We have gained insights with TCAD simulations on how to realize a graphene DEPFET.

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