Next-Generation Electronics by Co-Design with Chalcogenide Materials

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Abstract

As Moore's law approaches its limits, chalcogenides offer a promising route to next-generation computing and sensing, thanks to their topological, magnetoelectric, excitonic, and spintronic properties. Yet the very traits that make them appealing, e.g., exotic properties at monolayer thickness, clean van der Waals interfaces, and strong many-body effects, also heighten sensitivity to fabrication processes, causing issues that prevent the translation of novel material property into device functionality. This article examines key obstacles in controlling chalcogenide heterostructures and stresses the need for an integrated co-design strategy, spanning materials synthesis, processing, and device architecture, to unlock their potential. Successful solutions will enable transformative advances in spintronics, photonics, and quantum information systems.

Main Text

Moore's law[1], the semiconductor industry's guiding principle for over half a century, is ending. Similar statements have been made by researchers for many years, however, improvements in material quality and innovative fabrication techniques have repeatedly delayed the law's anticipated demise[2-5]. Nonetheless, physical limitations associated with shrinking device dimensions are now becoming unavoidable. Fundamentally, conventional electronics relies on shuttling charge through ever-smaller transistors, and beyond a certain scale, electrons cannot be reliably controlled without incurring unacceptable power losses and heat generation[6-10]. If computing technologies are to continue advancing, we must look beyond classical charge-based logic toward new paradigms that leverage other fundamental physical resources, such as spin or light, and reimagine how information is processed, stored, and transmitted. Quantum computing and neuromorphic architectures are prime examples of potential successors, but their realization hinges on harnessing quantum materials whose exotic quasiparticles can truly move us beyond the charge-manipulation framework. Due to the entangled nature of quantum resources and their sensitivity to local surroundings, we must also reimagine the co-design workflows to realize quantum technologies. Traditional Technology Readiness Levels (TRLs), even when applied to quantum technologies, still reflect linear trajectories from fundamental principles to practical applications[11,12]. However, to fully harness new quantum resources, we must recognize the intrinsic link between quantum material property and quantum device functionality and adapt a more end-to-end cyclic co-design process as shown in Fig. 1.

Over the past decades, there has been a surge of "use-inspired" research into novel quantum materials that promise remarkable properties for next-generation technologies. These materials, exemplified by chalcogenides and other two-dimensional (2D) systems, exhibit quantum phenomena such as excitonic and many-body interactions[13-18], topological order[19-22], magnetoelectric and multiferroic effects[23-26], and tunable bandgaps[27-30]. The foundational breakthroughs in isolating single-atom-thick layers of graphene spawned an avalanche of discovery across a broad family of 2D compounds[31]. Today, chalcogenides stand out in particular for demonstrating exotic phenomena, including superconductivity[32-36], ferromagnetism[37-39], and ferroelectricity[40-48], in atomically thin layers. These properties and phenomena are not simply academic curiosities: they open the door to entirely new device concepts, including field effect and spin-based transistors[49-58] and memories[59-66], spintronics[49,60,67-78], valleytronics[74,75,79-88], high-

performance optoelectronics and photonics[29,62,89-111], neuromorphic[65,112-121] and quantum computing platforms[90,122-133], and many others as outlined in Fig. 2. The central question becomes how to make the use-inspired useful.

Despite these impressive demonstrations of novel physics, efforts to integrate 2D chalcogenide materials into large-scale, commercial-ready devices have remained largely proof-of-concept. The crux of the challenge lies in translating exotic quantum properties into robust, manufacturable, and scalable platforms without quenching the very effects that make these materials so compelling. Traditional semiconductor processing techniques, developed and refined over decades for silicon and CMOS based technologies, often fail when applied to chalcogenides, either due to chemical incompatibilities, interface damage, or the introduction of parasitic defects[113,134-138]. Because 2D materials often rely on van der Waals bonding to maintain ideal, dangling-bond-free interfaces, conventional chemical etching, lithography, and thermal treatments can introduce inhomogeneities, impurities, and cracks that degrade device performance[113,135-145]. Furthermore, the inability to effectively dope 2D semiconductors in three-dimensional ways complicates forming reliable, ohmic contacts, which remain a critical bottleneck in making operational 2D circuits[136,144,145].

Yet it is precisely these ultra-clean, atomically sharp interfaces that make chalcogenide materials so promising. With no dangling bonds at the surface, 2D chalcogenides can be stacked in arbitrary heterostructures with relaxed constraints of lattice matching, resulting in tunable interfaces[64,94,141,146-152]. Their extended possibilities for phase and defect engineering allow for substantial control over physical properties, ranging from band alignments and carrier densities to magnetism and excitonic interactions, by adjusting the atomic and electronic structures on demand[92,113,147,153-160]. The potential for low-leakage, high-mobility devices at sub-nanometer gate lengths has generated enormous excitement[53,54,99,101,106,160-168]. Additionally, the dramatic range of bandgaps exhibited by these materials, encompassing metallic to semiconducting regimes, offers versatility in designing both logic elements and photonic devices for applications in data communications, sensing, and quantum information[27-29,58,92,168-176].

An equally important aspect is the potential energy efficiency gained by moving to 2D chalcogenides. The atomically thin nature and absence of dangling bonds reduces charge traps and short-channel effects, which together help curb power dissipation[53,58,64,92,177-180]. In emergent computing paradigms, such as neuromorphic and quantum computing, device density and low-latency operation are paramount and 2D chalcogenide materials are well-positioned to meet these requirements[113]. For instance, transistor and optoelectronic elements with large on/off ratios and floating-gate nonvolatile memory with extraordinary retention times have been demonstrated using ultrathin layers[59,101,160,166,181-183]. Similarly, functionalities based on ferroelectric and exciton-driven photodetection point to applications in integrated compute-sensor-memory systems capable of performing many co-located tasks in parallel[113,184-187]. These developments highlight how chalcogenide materials could allow complex information processing to occur directly where data is collected, fundamentally improving bandwidth, latency, and energy consumption.

Still, significant obstacles remain. The surface sensitivity of 2D materials necessitates advanced interface engineering so that gate dielectrics, metal contacts, and protective encapsulation layers do not introduce extrinsic defects or compromise their crystalline integrity. Equally pressing is the need for consistent, wafer-scale growth of chalcogenides with precisely controlled layer numbers. Although chemical vapor deposition (CVD) techniques have produced impressive monolayer crystals, controlling layer thickness across large areas remains challenging. Alternatives such as molecular beam epitaxy (MBE) and atomic layer deposition (ALD) combined with atomic layer etching (ALE) offer promising paths for achieving layer-by-layer control in a manner that integrates smoothly with existing CMOS infrastructure[113,188-192]. Recent review articles offer comprehensive assessments of chalcogenide synthesis methods, which fall outside the scope of this article[139,151,165,186,192-197]. Beyond wafer-scale synthesis, doping and defect engineering require a more systematic approach that correlates processing conditions with the resulting fundamental device characteristics, especially for quantum and neuromorphic applications, where localized defects can be both detrimental and potentially beneficial depending on their role in electron or spin transport.

Here our aim is to draw attention to the critical challenges, and research opportunities, in bridging fundamental chalcogenide quantum material research and practical device technologies. We first examine the central hurdles in interfacial materials physics, including the formation of clean, reliable interfaces, contacts and the management of defects. We then discuss current emerging nanofabrication strategies and the opportunities they present for scalable manufacturing, highlighting both successes and open questions in harnessing chalcogenides for spintronics, optoelectronics, and quantum information science. Our goal is not to provide an exhaustive survey, but to illustrate the breadth and novel behaviors of chalcogenide materials as they are transformed into functional devices. By illuminating these interconnected challenges, we aim to reveal research opportunities needed to accelerate the realization chalcogenide-based technologies. Ultimately, a concerted effort to refine growth processes, improve device architectures, and develop robust transfer and integration methods is necessary to realize the potential of these unique quantum materials. By systematically tackling these issues, we may unlock entirely new frontiers in computing and sensing, transcending the charge-based paradigm that has underpinned Moore's law, and ushering in an era where spin, light, and topology become essential resources for technological advancement.

Materials Interfaces – Challenges and Opportunities:

In his 2000 Nobel lecture, Herbert Kroemer famously stated that "the interface is the device," highlighting that the performance of semiconductor heterojunctions is often determined more by the properties of the interface than by the bulk [198]. This concept, dating back to the 1950s, revolutionized electronics and optoelectronics by enabling band-gap engineering in heterojunction transistors, semiconductor lasers, and advanced integrated circuits. This perspective remains highly relevant, particularly as we explore novel chalcogenide quantum materials. These materials can host a variety of exotic electronic and magnetic states, yet they present a new set of material science challenges for device fabrication. Among these challenges are understanding and controlling the interfacial structure, cross-interface coupling, and material diffusion. Below, we

discuss each of these aspects, highlighting recent insights and open questions in chalcogenide-based heterostructures.

Interfacial Structure

Chalcogenides such as the transition-metal dichalcogenides (e.g., $NbSe_2$, $TiSe_2$) and tetradymite topological insulators (e.g., Bi_2Te_3, Bi_2Se_3) can form a variety of interface structures when layered together or when integrated with other materials. In traditional semiconductors, small lattice mismatches or differences in atomic arrangements at interfaces can cause defects, reconstructions, or strain that modifies electronic transport[199-202]. With chalcogenides, these effects can be even more pronounced. In many cases, the interlayer van der Waals forces relax lattice matching conditions which suggests promising routes towards tailored device structures[94,149,150]. However, interfaces between atomically similar chalcogenide materials may undergo reconstructions or form interfacial defect layers, whereas interfaces that bridge different symmetries can, at times, be strikingly abrupt. For instance, as shown in Fig. 3 the interface of tetragonal superconducting Fe(Te,Se) grown on hexagonal Bi_2Te_3 or MnTe can be atomically sharp [203-205], while the $NbSe_2/Bi_2Se_3$ interface can exhibit a misfit layer with a distinct structure [206]. Such subtle differences have profound implications for functionality: the former may preserve high mobility or coupling between quantum states more readily, whereas the latter can create dead layers that may hinder desired proximity effects.

These contrasting outcomes reveal a zoology of interface and defect structures, from interfacial phases, to reconstructions, to well-ordered junctions, and each variant can dramatically alter properties relevant to functional devices. Deeper investigations are required to unravel the mechanisms and energetics governing interfacial structures and to establish clear causal links between interfacial properties and device performance. For example, defects, interfaces and grain boundaries can be problematic for carrier mobility, magnetic ordering, and excitonic lifetimes critical for neuromorphic applications[113], while, atomically sharp interfaces between functional layers facilitate long-term data retention in non-volatile floating gate memory devices[59]. Controlling magnetic dead layers is critical for spin-orbit torque based magnetic switching in memory devices, however, control over interfacial symmetries can also dramatically improve performance of magnetism-based applications[60,207,208]. Hence, a key research avenue is understanding how to systematically tune these interface structures in scalable platforms and architectures to functionalize the desired exotic states. The ultimate goal is to trace the causal chain from interfacial structure to materials properties and, ultimately, device performance. However, more systematic studies are needed to discern whether these relationships follow universal rules or are system-specific.

Cross-Interface Coupling

Once an interface is formed, a second challenge lies in the electronic, magnetic, excitonic, and phononic couplings across the boundary. Charge transfer, band alignment, and the emergence of collective modes are all affected by the local environment at the interface. For example, charge transfer across a MoS_2 and WSe_2 heterojunction leads to a photoelectric effect with excited excitons controllable by interface engineering[92,209], while band alignments can be controlled by chalcogenide stacking configuration and twist angles[96,210,211]. In addition, work function differences between materials are vital for forming ohmic contacts in device structures[140].

For chalcogenides, these interfacial couplings can shape excitonic properties. With strong Coulomb interactions and reduced dielectric screening leading to large exciton binding energies, chalcogenide heterostructures enable room-temperature excitonic devices and high absorption for photodetection and optical devices over a wide range of band gaps[13,212-216]. When the work functions of adjacent layers differ or the dielectric screening at the interface changes significantly, excitons may localize in specific layers or form strongly bound interlayer complexes[217-223]. Tuning these interfacial properties thus provides an additional degree of freedom for quantum sensing and optoelectronic devices.

The cross-interface coupling of different degrees of freedom can lead to exotic states and dramatic enhancement of exotic quantum properties of technological interest. The interface of a topological insulator and even parity superconductor can yield Majorana bound states, whose non-Abelian statistics and degenerate states topologically protected from local perturbations could be utilized for fault tolerant quantum computations[125,133,224]. Another striking example is monolayer FeSe grown on $SrTiO_3$ where charge transfer combined with the interaction between FeSe's 2D electronic structure and $SrTiO_3$'s high-energy optical phonons enhances the superconducting transition temperature far above its bulk value[32,33,225]. Similarly, in magnetic topological insulators like $MnBi_2Te_4$, the interplay between bulk antiferromagnetic layers, surface topological bands, and termination-dependent magnetization yields unusual hysteresis loops and even-odd layer–dependent axion and Chern insulator phases as well as exchange bias effects in device structures[226-230]. It has also been shown that the effective thickness in this even-odd dichotomy depends on fabrication processes for device structures[231].

The preceding example underscores the remarkable diversity of phenomena that emerge from cross-interface coupling, yet a unified framework for predicting and controlling these effects is still lacking. Advancing the field will require systematic efforts to clarify how cross-interface interactions are governed, and how they evolve under different nanofabrication processes.

Diffusion

A final, but equally critical, challenge in building chalcogenide-based heterojunctions is controlling diffusion across interfaces as outlined in Fig. 4. During material synthesis and device fabrication, cross-interface diffusion can degrade or, counterintuitively, enhance properties. Many traditional metals used for contacts in semiconductor device fabrication have been observed to chemically react and diffuse into chalcogenide materials[232]. Such diffusion can also be used to influence spin-orbit torques for manipulation of magnetic layers[233]. The van der Waals nature of this class of materials yields highly anisotropic diffusion pathways that can affect the material phases and resulting contact resistance[234,235]. Taking advantage of these anisotropic pathways may open an avenue for creating phase engineered interfaces with tailored contact resistances[236].

However, the cross-interface diffusion of materials can also generate new materials, properties or alter functionality of devices. For example, as shown in Fig. 4d, diffusion of Pd into $(Bi,Sb)_2Te_3$ may induce a topological superconducting phase potentially relevant for the creation of Majorana zero modes and quantum computing applications[237,238]. Similarly, the diffusion of Te across the $Fe(Te,Se)/Bi_2Te_3$ boundary can enhance superconductivity of the heterostructure, potentially making Majorana zero modes more accessible for device applications[205]. On the other hand,

unintentional diffusion may introduce impurities or adatom defects that trap charge and act as scattering centers known to degrade carrier mobility[134,142,167,177,239-242].

An extreme illustration of the impact of diffusion is the growth of $TiSe_2$ by simply evaporating Se onto a heated TiO_2 substrate as shown in Fig. 4e,f. The Ti effectively migrates out of the oxide layer, forming a chalcogenide film with the same atomic and electronic structure as bulk $TiSe_2$[243]. These examples underscore the double-edged nature of diffusion: it can be harnessed for device engineering but must be precisely understood and regulated. Going forward, systematic studies of diffusion pathways, barrier materials, and controlled doping profiles are crucial for reproducible high-performance and scalable device platforms based on chalcogenide heterojunctions.

Herbert Kroemer's message continues to hold as we look beyond traditional semiconductor technologies. For chalcogenide quantum materials, the interface remains the core platform where exotic electronic, magnetic, and topological states can emerge, or be quenched. Although our focus centers on interfaces within the active chalcogenide layers, the same issues extend to encapsulation and passivation layers. Researchers commonly use materials as Se, Te, FeTe, AlO_x, h-BN, Al_2O_3, etc., as provisional capping layers for materials characterization and device structures[244-247]. However, systematic efforts to engineer passivation layers that both safeguard key properties and remain compatible with device fabrication are underdeveloped.

To harness the diverse properties of chalcogenides the interfacial structure, cross-interface coupling, and diffusion, must be mastered to develop next-generation devices. With continued effort, these avenues will pave the way to breakthroughs in novel topological electronics, spintronic, and optoelectronic architectures that extends beyond the boundaries of Moore's law for next generation quantum technologies.

Device Fabrication – Challenges and Opportunities:

As discussed, chalcogenide materials exhibit exotic quantum properties with tremendous potential for use-inspired applications. Beyond understanding and controlling material interfaces, it is crucial to address the practical realities of integrating these sensitive quantum systems into scalable device architectures. While device fabrication is commonly viewed as an engineering task, many of the fundamental scientific principles underlying fabrication approaches for novel quantum materials remain unknown and underexplored. Significant questions regarding behavior of sensitive materials to energetic physical and chemical processing during nanofabrication and integration are of growing concern. Here, and highlighted in Fig. 5, we examine common pitfalls arising when traditional fabrication techniques are applied to low-dimensional chalcogenides, alongside mitigation strategies and novel approaches for translating the promise of exotic quantum states into scalable quantum technologies. For quick reference, a practical guide to common issues and possible solutions for each nanofabrication technique discussed below is presented in the Supplemental Information[248].

Lithography

In today's device fabrication, e-beam and optical lithography are crucial for defining device features as outlined in Fig. 5a. Polymer resists (e.g., PMMA, EL, AZ, SPR) are coated onto substrates, baked (e.g., at 90 °C–200 °C), exposed, developed, rinsed, and dried, with optional post-exposure or hard

bakes as needed. The resulting photoresist pattern then serves as a mask for subsequent processing. Applying these methods to chalcogenides requires careful consideration, as repeated exposure to aqueous developers (e.g., 2–3% TMAH) and organic solvents, alongside multiple heating/cooling cycles, can cause thermal degradation or introduce residual stress. Moreover, as shown in Fig. 5b, widely used e-beam and optical resists often leave organic residue that can impede lift-off, degrade surface characterization, and introduce non-uniform charges at metal–sample interfaces[249]. This residue can unintentionally dope materials and reduce mobility[250,251], create trap states that lower photocurrent[252], and block key phenomena in low-dimensional systems[253]. Although PMMA generally leaves less residue, complete removal remains difficult; time-of-flight secondary ion mass spectrometry confirms its persistent presence on 2D materials[254].

A critical step in both photolithography and electron-beam lithography is the resist pre-bake. Photolithographic resists are usually baked near 100 °C, whereas standard e-beam resists require ≈180 °C. This bake removes residual solvent, anisole in the case of PMMA, before exposure. Solvent trapped during development blurs feature edges and limits aspect ratio, so the benefit of an effective bake increases as the critical dimension shrinks.

Chalcogenide materials, however, are unusually temperature-sensitive. Even moderate baking (~100 °C) accelerates chalcogen loss because of their high vapor pressures, and brief excursions to ≈200 °C can oxidize the chalcogen species. During molecular-beam epitaxy, practitioners compensate for this volatility by providing an excess chalcogen flux[194,255]; during pre-bake, by contrast, the same volatility drives chalcogen loss, creating vacancies and other defects[256]. For 2D chalcogenides, the effect is amplified at nanoscale dimensions, where vacancy formation quickly pushes the film off-stoichiometry[195,257-262]. These defects degrade the electronic and quantum properties of many chalcogen-based materials, including topological insulators, lowering carrier mobility, destabilizing phases, and reducing Hall mobility[263,264].

Consequences are still more severe for chalcogenide superconductors such as Fe(Te, Se): off-stoichiometry introduced during resist baking can suppress the critical temperature or quench superconductivity altogether by introducing percolative normal-resistance paths[265,266]. Mitigation strategies therefore focus on minimizing thermal load—lowering bake temperature and time, omitting the bake entirely, or performing it in an inert atmosphere to eliminate oxidation. These approaches preserve chemical integrity at the expense of lithographic fidelity, often yielding blunter sidewalls. Ultra-thin chalcogenide films are especially vulnerable, whereas non-chalcogenide quantum-material platforms generally tolerate the modest heat budgets typical of resist baking.

Thermal annealing above 300 °C in argon, hydrogen, forming gas, or vacuum[267-269] is widely used for residue removal. However, many chalcogenides degrade at this temperature, which is above their synthesis temperature, and annealing alone may not suffice[254,267]. Elevated temperatures can also introduce defects, unintentional doping, and oxidation; vacuum annealing may boost carrier mobility but risk generating amorphous carbon and additional defects[270,271]. In sulfide-based chalcogenides, annealing frequently induces sulfur vacancies[272,273]. Plasma treatments and wet cleaning with heated solvents have proven effective in traditional semiconductors[274-279], but reactive plasma often introduces defects in 2D metal chalcogenides[280]. Alternatives such as contact atomic force microscopy (C-AFM)[250,281], electron beam treatment[282], and light-based treatments[283] have shown promise for MoS_2, WSe_2, and graphene, though broader validation is

needed for other low-dimensional systems. Ultimately, residue removal must balance cleaning efficacy with minimal damage, especially critical for chalcogenides prone to oxidation and thermal degradation. As lithographic techniques dominate device foundries, systematic study of these approaches in chalcogenides remains a vital yet underexplored need.

Wet Etching

Wet etching is performed by immersing the sample in a reactive solution that dissolves or vaporizes by-products, making it one of the most straightforward and economical methods for material removal. This process can create complex structures unattainable by other etching techniques, particularly those requiring controlled under-etching for suspended patterns[284,285]. Another major advantage is its high selectivity: carefully formulated and optimized acids, bases, or mixtures can remove a specific layer in a multilayer stack without affecting other layers.

As shown in Fig. 5c, principal drawback is that wet etching is often isotropic, leading to significant undercutting below the mask[286]. This undercut can be exacerbated when the mask lifts slightly near the feature opening. Although pre- and post-baking of resists, judicious etchant selection, and fine-tuned process parameters can mitigate undercutting, it cannot be entirely avoided, making wet etching more suitable for larger features. Another key parameter is the etch rate, which can be controlled by optimizing the etchant concentration or solution temperature to improve precision.

Wet-chemical etching is a standard route for patterning layered chalcogenide films such as Bi_2Se_3, Bi_2Te_3, (Bi,Sb)Te, and (Bi,Sb)(Te,Se)[287-290]. These compounds, celebrated as topological insulators, have enabled a decade of device studies aimed at dissipation-free spintronics that exploit spin–momentum locking. Common mineral acids, HCl, HNO_3, H_2SO_4, and HF, readily etch the films, yet when used full-strength they attack so aggressively that severe under-cutting is routine. Diluting the acid with H_2O_2, de-ionized H_2O, or mild organic acids lengthens the etch time and sharply reduces under-cut formation.

Mercury-based chalcogenides pose different chemistry. HgTe thin films, for example, are etched with a KI/I_2/HBr mixture diluted in water; the I_2 concentration sets the etch rate[291,292]. Magnetically doped topological-insulator films are often processed in a gentler bath of $H_3PO_4/H_2O_2/H_2O$, which gives a more controllable, intermediate rate.

Photoresist or e-beam resist generally serves as the etch mask and yields well-defined features. When still tighter control is required, a hard mask such as ALD-grown Al_2O_3 can be substituted; the hard mask is then removed in a separate, selective step[293] . Although effective at suppressing under-cutting, this option lengthens the process flow.

Highly anisotropic, hexagon-edged etches have been demonstrated on transition-metal dichalcogenides (WS_2, MoS_2, $MoSe_2$) using a $NH_4OH/H_2O_2/H_2O$ solution[294,295]. Patterning of Bi_2Te_3/FeTe heterostructures, candidate topological superconductors, has been achieved with an $HCl/H_3PO_4/H_2O$ mixture[296].

If the etch proceeds too slowly, a modest temperature rise (≈60–70 °C) can accelerate the reaction without inducing excessive under-cutting. Post-baking the resist likewise suppresses under-cutting by hardening the mask, but any thermal step must be used judiciously for chalcogenides, where heat promotes chalcogen loss and sample degradation.

Perhaps the greatest virtue of wet etching is its chemical selectivity: properly chosen chemistries can remove a chalcogenide layer cleanly while leaving neighboring non-chalcogenide layers untouched, enabling sophisticated heterostructure devices with minimal collateral damage. However, more efforts are needed to understand chalcogen specific etching chemistries.

Despite these challenges, wet etching remains a vital technique due to its simplicity, cost-effectiveness, and high selectivity. By selecting appropriate etchants, refining process conditions, and employing robust masking strategies, it can be successfully applied to numerous fabrication scenarios. As shown in Fig. 5d, to unleash the power of chalcogenide materials, suitable wet etching chemistries are indispensable and needs further investigation. Fundamental chemistry and materials science investigations of etchants to improve chalcogenide selectivity while maintaining compatibility with traditional semiconducting material processes remains a critical gap.

Reactive Ion Etching

Reactive ion etching (RIE) is a plasma-based technique used to pattern materials during micro- and nanofabrication. Reactive ions generated in a plasma physically sputter or chemically react with select materials, forming volatile byproducts. The degree of directionality (anisotropic vs. isotropic) and selectivity is influenced by chamber pressure, gas flow rates, gas choice, and temperature.

Reactive-ion etching (RIE) of chalcogenide films is typically carried out with fluorine- or chlorine-based plasmas; common feed gases are SF_6, CHF_3, Cl_2, and BCl_3 [297-301]. Etching proceeds through the strong chemical affinity of F^- and Cl^- radicals for the constituent elements. Layered transition-metal dichalcogenides (MoS_2, $MoSe_2$, WS_2, WSe_2) and topological chalcogenides (Bi_2Se_3, Bi_2Te_3, $MnBi_2Te_4$, WTe_2) are readily patterned in an SF_6 plasma. Raising the RF power accelerates removal of thick films, but at the cost of enhanced chalcogen volatility, which can degrade device performance. A standard workaround is to admix a small fraction of Ar (≈1 : 10 Ar : F/Cl gas). The heavier Ar^+ ions provide a complementary physical sputter component, dislodging surface atoms while the F/Cl species perform the chemical step; the combined mechanism shortens the required plasma exposure and limits thermal damage.

Poor selectivity is the principal limitation of RIE. Halogen plasmas etch most materials, including gate dielectrics and metals, albeit at different rates, so precise knowledge of those rates is essential. They can vary with chamber geometry, pressure, and power density, meaning each tool must be calibrated individually. When chalcogenide heterostructures are involved, practitioners often lower the etch rate to achieve a clean stop at the intended interface; yet the slower recipe increases the risk of over-etching and roughening adjacent layers. In this respect RIE contrasts with wet-chemical methods, where the reaction ceases automatically once the targeted layer is removed, preserving the underlying stack in chalcogenide devices.

RIE of chalcogenides can be problematic because these materials are highly sensitive to damage and contamination. Ion bombardment can break bonds, resulting in defects, amorphization, and stoichiometry changes—particularly in transition metal chalcogenides, where lighter atoms may be preferentially sputtered[261,302-304]. This can be particularly problematic for devices where the ‘cut’ edge of the material forms the active device region. Residual ions and etch byproducts (e.g., reactive F or Cl species) can introduce unwanted dopants and alter intrinsic properties. As a solution, one can rinse with a wet-etchant to remove byproducts produced during the RIE process.

Importantly the wet-etchant must be dilute enough so that it does not cause undercutting as discussed in the previous section. The choice of masking materials is also critical for minimizing damage.

RIE is highly energetic, it can cause thermal damage to low-melting-point materials or generate additional defects at elevated temperatures. Although studies RIE-induced defects in Bi_2Se_3, $Ge_2Sb_2Te_5$, WSe_2, and $MoSe_2$ exist[304-306], there is a pressing need for more systematic investigations to fully understand the implications of these defects at the device-level[305].

Defect formation is best curbed by running the plasma at lower RF power. With reduced power the ions strike the surface with less energy, generating less Joule heating and thereby preserving film stoichiometry, suppressing RIE-induced defects, and minimizing roughening of underlying layers. Actively cooling the substrate stage, typically with a liquid-nitrogen loop or chilled water, adds a further thermal buffer. These precautions are especially critical for chalcogenide films, whose weak bonding leaves them highly vulnerable to heat-driven damage.

Moreover, RIE can affect underlying layers when overetching is required to ensure complete removal of the target layer. Such overetching often exposes the layer beneath to roughening, contamination, or other modifications.

Alternatives to conventional RIE include chemical etching, low-power chemically selective RIE, and ALE[307-309]. The choice of masking materials is also critical for minimizing damage. ALE, like ALD, involves cyclical exposure of the material to a reactive precursor (which modifies the surface), followed by the removal of that modified surface using low-energy ions or thermal energy, one atomic layer at a time. Although it can be time-consuming, ALE is ideal for atomically thin dichalcogenide materials because it reduces unwanted damage and preserves underlying layers. Although ALD has been well-established for some time, the application of ALE specifically to chalcogenides is a more recent development. ALE has been shown to be more effective than RIE for etching materials such as MoS_2 and WSe_2, achieving precise etching with minimal defect formation and surface roughness. It is important to note that when utilizing ALE, the temperature of the sample holder should be kept as low as possible, as elevated ambient temperatures (typically above ~80°C) are generally required to facilitate reactions within the ALE chamber. Recent reviews highlight the breadth of materials processed by ALE[310], but further investigation is needed for reliable and scalable chalcogenide processing.

Focused Ion Beam Milling and Direct Write Processing

Focused ion beam (FIB) milling is a versatile technique for nanofabrication, modification, and characterization at the nanoscale. Ion beams are formed by extracting ions from an ion source (e.g., generated by plasma, field evaporation of liquid metal, or gas field ionization), which are subsequently accelerated (commonly 200 V–50 kV) and electrostatically focused into a nanoscale probe that is scanned deterministically across the sample[311]. The key advantage of FIB is that ions can transfer energy via elastic collisions, displacing or sputtering target atoms or implanting ion species, thereby altering the topography, structure, and chemistry of the target, without requiring the resists or etchants used in photo/e-beam lithography. As such, the so-called direct-write FIB process is particularly attractive for patterning environmentally and process-sensitive materials such as metal chalcogenides. Moreover, this approach greatly reduces contamination from organic

residues. However, the high ion energies generate collision cascades in the target material, leading to damage and amorphization that can extend well beyond the beam's incidence point. The extent of this delocalization and damage depends on factors such as the target material, ion species, ion energy, and incidence angle[312].

Conversely, introducing defects during FIB irradiation can be detrimental, sometimes outweighing the advantages it offers over standard lithographic approaches. High-energy ions generate vacancies, interstitials, and even amorphous tracks in the target lattice[313]. In Pb-based chalcogenides the beam can trigger local phase transformations in the material surrounding the impact zone[314]. Irradiation also produces intense, localized heating; because chalcogenide bonds are comparatively weak, these thermal spikes can exceed the bonding energy, sever bonds, and dramatically degrade electrical properties[315]. The resulting defect cascades and redeposited material can spread laterally over tens of micrometers, undermining neighboring regions and complicating the fabrication of micron-scale chalcogenide devices[316-318]. The risk is especially acute for chalcogenide superconductors: damage propagated by the beam tail or by sputtered ions reacting with residual gas can irreversibly suppress superconductivity in areas far beyond the intended write zone. Such is the case for FIB processing of chalcogenide thin film materials, as shown in Fig. 7. Direct milling of 10 nm Fe(Te,Se)/50 nm Bi_2Te_3 microstructures with Xe^+ ions at high current (2 μA) destroyed superconductivity—likely due to sidewall damage and beam-induced amorphization propagating across a 10 μm-wide channel.

Thus, one needs to optimize the beam species as well. Ga^+ beams have long been used to create planar Josephson junctions and superconducting quantum interference devices[319-323]. Plasma FIB (PFIB) systems further increase throughput by removing larger volumes more rapidly, while also offering the flexibility to select an ion species and mass that optimize elastic collisions with noble gas ions (Xe^+, Ar^+) or introduce inelastic processes through reactive species (O^+, N^+). High-resolution gas field ionization provides high brightness and resolution with lighter ions (He^+, Ne^+), enabling sub-10 nm patterning resolutions with inert species and reduced ballistic damage[324,325]. However, even these lighter ions can cause implantation, defect formation, and surface roughness, thereby affecting crystallinity, electrical properties, and magnetization (e.g., via domain wall pinning)[326]. Nonetheless, the impact of ion-induced defects is context-dependent: recent years have seen growing interest in defect engineering via the spatial precision and controlled defect introduction possible with FIB, particularly with He^+ ions[327,328]. Low temperature post annealing can be effective in healing some of the defects caused by ion irradiation. Another critical strategy is to minimize the beam energy and current during irradiation. Utilizing low beam currents, such as around 10 pA, and lower voltages (approximately 20–30 kV) has been shown to cause minimal or even negligible damage to chalcogenide-based topological insulators. It is advisable to begin with a higher beam current and energy for initial etching, which allows for the efficient removal of larger portions of the material and reduces overall thinning time. As the process approaches the final device channel, both the beam energy and current should be significantly lowered (to around a few pA and approximately 5 kV) to minimize damage.

Whether the goal is to introduce defects or to avoid them, a deeper understanding and better predictability of the effects of ion species, energy, reactivity, flux, fluence, and reactive precursor gases are essential moving forward.

Electrical Contacts

Electrical contact regulate charge flow from the metal electrode to the device channel. Contact resistance arises at the interface of dissimilar materials, stemming from energy-band discontinuities that disrupt charge transport[144]. To maximize device performance and minimize contact resistance, there are two important factors: (1) doping mismatch, where substantial differences in doping levels raise contact resistance; and (2) contact area, where a smaller area can induce "current crowding." The current crowding effect can be significantly mitigated through the edge contact method. In this approach, the transition metal dichalcogenide (TMD) is first coated with an insulating layer, followed by a patterned etching step that exposes the edges of the layered structure for metal contacts. This edge contact configuration allows charge carriers to flow laterally into each layer of the chalcogenide, facilitating smaller device sizes. Consequently, this scaling down enhances device density, an essential factor for industrial scalability. Contact resistance is typically measured using four-probe methods, Kelvin probe, or Transmission Line Models[329,330]. Metal selection is also crucial. For traditional semiconducting materials Cr and Ti often form ohmic contacts due to their low work functions and strong adhesion, while Pt and Ni generally create Schottky contacts. For many chalcogenides, these conventional metals may chemically react or diffuse into the material[232,234,235]. For example, despite its higher work function, Pd often achieves relatively low contact resistance but can also form tellurides and selenides at room temperature and thus alter the work function[144,238,331]. The peculiar properties necessitate the exploration of new contact materials or alternative approaches such as phase-engineering[236]. Au is widely regarded as forming an excellent Ohmic contact with chalcogenides compared to other contact metals. However, it is important to note that the adhesion of Au to chalcogenides is relatively poor. Recently, antimony (Sb) has been observed to exhibit extremely low contact resistance when deposited on MoS_2. Additionally, indium (In)/gold (Au) contact has demonstrated minimal contact resistance after annealing at 200°C on transition metal dichalcogenides (TMDs) such as MoS_2 and WS_2[332]. These materials show promise as future contact options for ultralow contact resistance electronic devices.

There are several strategies to reduce contact resistance. It has been predicted and experimentally shown that insertion of a single layer of hBN between chalcogenide and metal significantly drops the contact resistance or the Schottky barrier height by reducing the interaction between the metal and the sample. Graphene has been demonstrated to enhance the TMD device performance when it is inserted between MoS_2 and Ag contact[333]. Controlled annealing has been shown to improve the metal-semiconductor adhesion but must be carefully managed to avoid thermal degradation of chalcogenide materials or harmful interfacial diffusion. Additional methods, such as carbide formation or carefully patterned contacts, further decrease contact resistance with materials like graphene[334,335], although again, one must remain aware of chalcogenide stability at elevated temperatures. Another concern is wetting where metals with high surface energy can form islands rather than continuous films on certain substrates, a challenge partly addressed by selective surface passivation[336]. Another innovative strategy that has recently emerged is the mechanical transfer of metal pads onto 2D chalcogenides[337]. In this approach, metal pads are pre-patterned and then transferred onto the chalcogenide layer with the assistance of polymer materials such as PMMA or PDMS. This method has demonstrated a significant reduction in contact resistance by several orders of magnitude.

Contact formation by metal deposition is a critical step in chalcogenide-device fabrication[338]. Because 2D chalcogenides are only a few atomic layers thick, they are far more vulnerable to process-induced damage than bulk silicon, the mainstay of conventional microelectronics. Sputtering and electron-beam (e-beam) evaporation are the two methods used most often. During e-beam evaporation the arriving atoms carry ~0.1 eV of kinetic energy, whereas sputtered species arrive with 10–100 eV. The gentler bombardment in e-beam evaporation yields smoother, sharper metal/chalcogenide interfaces with minimal intermixing or interdiffusion, and thus less damage to the underlying crystal. For that reason, e-beam evaporation is generally preferred for layered chalcogenides. Contact quality improves still further when the metal is deposited in an ultrahigh-vacuum environment, which suppresses contamination and oxide formation.

Solid-phase epitaxy is especially relevant to layered chalcogenides as shown in Fig. 6, where Pd or Pt can react to form superconducting compounds ($Pd_{1-1.1}Te$, $PdTe_2$, $Pd_{6-7}Se$, and Pd_4Se) with transition temperatures up to about 4 K[339]. Remarkably, these reactions may occur at room temperature or with mild annealing, yielding highly transparent contacts on topological semiconductors—some with Josephson junction transparencies near 0.96[237,340,341]. Although largely self-limiting, such reactions can still show lateral metal migration up to tens of nanometers, complicating device design.

Ultimately, achieving low contact resistance in advanced materials, quantum or otherwise, requires balancing doping, contact geometry, interface cleanliness, and controlled solid-phase reactions. By managing these variables, it becomes possible to maintain stable, low-resistance interfaces that preserve the intrinsic properties of emerging material systems but requires coordinated feedback between materials development and fabrication development.

Lift-off

Lift-off is a common process used for adding materials, selectively, to regions where photoresist has been removed. It is commonly used to pattern metal traces and pads to make electrical contacts across a sample. During lift-off, a material, typically a metal, is deposited across substrates that have been coated with photoresist and lithographically patterned. Following metal deposition, the entire substrate is placed in a chemical bath that removes the photoresist and leaves the deposited material remaining in the areas that were not masked by photoresist. It is a good alternative to etching metals because it prevents the underlying material from being exposed to harsh chemical etchants or the higher temperatures or reactive plasma of a reactive ion etcher. While a potentially gentler alternative to etching, poor lift-off can cause shorts or missing regions, undermining device performance. As schematically shown in Fig. 5e, common issues include residual photoresist under the metal, unintended bridging where metal spans masked and unmasked regions, and poor metal-substrate adhesion, all of which can lead to unwanted detachment[331]. To prevent these pitfalls, one typically removes resist residue before metal deposition (e.g., via brief etching), employs bilayer resists for undercuts, and roughens the substrate with plasma treatments to enhance adhesion. Brief etching is an effective technique for achieving optimal lift-off during the fabrication process. Typically, O_2 plasma is used to remove residual organic components left over from lithography. However, the use of O_2 plasma is not recommended for chalcogenides, as these materials are highly susceptible to oxidation due to the energetic oxygen ions. Instead, inert gas plasmas, such as argon (Ar) ion plasma, are preferred for

this process. It is also crucial to operate at very low power when generating the plasma, and the etching duration should be kept minimal, generally around one minute, to prevent damage to the chalcogenide layers.

Adapting standard fabrication protocols remain critical for developing devices using quantum materials, yet alternative methods can reduce polymer residue. For instance, shadow or stencil lithography can form sub-micrometer contacts without resist[342], though precise alignment, potentially achieved via flip-flop chip bonders, is needed for multiple patterning. Another strategy relies on selective adhesion, where metal-coated or SAM-treated (self-assembled monolayer) regions of a quantum material exhibit stronger bonding. Transferring these regions onto patterned substrates, then flipping them to expose pristine surfaces, allows device fabrication with minimal metal and SAM contamination[343].

Outlook

Despite the challenges for functionalizing chalcogenide-based materials, recent developments show exciting progress towards scalable technologies. Progress in synthesis methods demonstrates that chalcogenide growth can be engineered at large scale and low temperatures, aligning with the stringent thermal budgets and CMOS processes. MOCVD strategies, for instance, have yielded wafer-scale crystalline films in mere minutes, controlling layer numbers from one to five while maintaining uniformity[189,190]. Likewise, strain engineering with silicon nitride capping layers has been shown to boost device performance, and the feasibility of solution-processed 2D materials points to future monolithic 3D memory–sensing–computing platforms[181,186]. Synthesis approaches using graphene or hexagonal boron nitride membranes also suggest novel approaches for synthesizing materials in specific device structures, thus avoiding many fabrication pitfalls[269,344]. Such achievements highlight the promise of integrating chalcogenides into industrial scale technologies, but they also underscore the need for precise end-to-end control over defects and interfaces to enhance electronic properties critical for functional quantum devices.

Maintaining quantum properties during processing is critical for quantum technologies and recent patterning and fabrication innovations have demonstrated fine-tuning quantum device structures. Phase engineering showcases how controlling stoichiometry, and crystalline phases can achieve abrupt low-resistance contacts and even superconducting states on demand[145,160,236]. Photoreactive crosslinkers also show promise for creating patterned device networks without the need for photoresist[345]. These on-device strategies circumvent the complexities associated with transferring 2D layers between disparate substrates, with the potential for paving the way for more stable, reproducible devices at the atomic scale. Meanwhile, lower-energy electron beam lithography protocols are reducing damage in chalcogenide materials, demonstrating that even delicate quantum materials can be integrated into nanoscale circuits using traditional fabrication tools without compromising their unique electronic states[346]. Complementary techniques, such as adhesion lithography, further boost yield by capitalizing on differences in interfacial adhesion energies to define device geometries without harsh chemical processes[343].

Finally, recent device architecture research underscores the strategic transition from transistor scaling to in-memory computing and other data-intensive paradigms. Large-scale integrated vector–matrix multipliers show that wafer-scale, high-yield arrays of floating-gate field-effect

transistors are now within reach, supporting advanced signal processing and neural network applications [347]. Concurrently, next-generation 2D transistors are approaching theoretical performance limits, hinting at the possibility of ballistic transport, low contact resistance, and quantum effects dominating device operation are on the horizon[348]. Yet critical gaps remain, e.g., dielectric integration, contact optimization, and wafer-scale uniformity, which hamper the widespread adoption of 2D chalcogenides for high-performance logic and quantum circuits[84,349]. Overcoming these hurdles will require coordinating end-to-end concerted efforts for understanding how to translate exotic quantum properties into functional devices ultimately position chalcogenides as a cornerstone of future quantum technologies.

Conclusions

As the impending end to Moore's law approaches, we must explore paradigms beyond traditional electronics. Two-dimensional chalcogenides, featuring clean van der Waals interfaces, exotic electronic and magnetic phases, and remarkable excitonic and spin-dependent phenomena, offer enhanced performance and new functionalities for quantum, neuromorphic, and photonic applications.

Yet the same qualities that make chalcogenides appealing, such as atomically thin layers, dangling-bond-free interfaces, and strong many-body interactions, render them fragile under traditional fabrication methods. Processes like lithography, wet etching, or ion milling can degrade mobility or quench quantum states, while interface diffusion can be exploited for new functionalities or unintentionally compromise device performance.

Realizing this potential requires a reimagined co-design approach with end-to-end integration of materials growth, interface engineering, patterning, and device architecture to recognize the inherent sensitivity of quantum states across multiple length scales. In the quantum world, defects and environmental conditions can affect desired device functionality in ways different from classical devices using more traditional semiconducting and CMOS material systems. Systematic studies are needed to understand how quantum material property and device functionality are interlinked and how fabrication processes affect this translation. Such endeavors require community level engagement with collaborations across materials science, engineering, physics, and chemistry to develop scalable workflows that preserve quantum properties.

Ultimately, 2D chalcogenides promise far more than incremental transistor improvements. By harnessing control over spin, light, topology, and excitonic interactions, they enable new classes of devices, from spintronics and valleytronics to fault-tolerant quantum circuits, transcending the limits of classical electronics. However, the entangled nature of quantum systems prohibits a simple separation of synthesis and fabrication processes and systematic attention from material interfaces, trough integration and prototyping, must be paid for these materials to usher in quantum technologies that can truly move us beyond Moore's law.

Acknowledgements

This material is based upon work supported by the U.S. Department of Energy, Office of Science, National Quantum Information Science Research Centers, Quantum Science Center. STR, SJR,

and SG are supported by the Center for Nanophase Materials Sciences, which is a Department of Energy, Office of Science User Facility at Oak Ridge National Laboratory.

Author Contributions

R.G.M. conceived the article. All authors discussed the concepts and D. M. and R.G.M. drafted the article. A. -H. C., Q. L., and M. B., contributed to the materials sections. S. G., J. L., J. Y., S. J. R., S. T. R., G. E., Y. P. C., and L. P. R. contributed ideas and text for the device fabrication sections. All authors reviewed the manuscript.

Competing Interests

The authors declare no competing interests.

***Additional Information**

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References

1. Moore, G. E., Cramming More Components onto Integrated Circuits, *Electronics* **38**, 114 (1965).
2. Rudolph, P. and Jurisch, M., Bulk growth of GaAs An overview, *J. Crys. Growth* **198-199**, 325-335 (1999).
3. Bohr, M., The evolution of scaling from the homogeneous era to the heterogeneous era, *IEDM Tech. Dig.*, 1.1.1-1.1.6 (2011).
4. Auth, C. *et al.*, A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors, *2012 Symposium on VLSI Technology (VLSIT)*, 131-132 (2012).
5. Salahuddin, S., Ni, K., and Datta, S., The era of hyper-scaling in electronics, *Nat. Electron.* **1**, 442-450 (2018).
6. Pop, E., Sinha, S., and Goodson, K. E., Heat Generation and Transport in Nanometer-Scale Transistors, *Proceedings of the IEEE* **94**, 1587-1601 (2006).
7. Kuhn, K. J., Considerations for Ultimate CMOS Scaling, *IEEE Transactions on Electron Devices* **59**, 1813-1828 (2012).
8. Frank, D. J., Power-constrained CMOS scaling limits, *IBM J. Res. Dev.* **46**, 235-244 (2002).
9. Haron, N. Z. and Hamdioui, S., Why is CMOS scaling coming to an END?, *2008 3rd International Design and Test Workshop*, 98-103 (2008).
10. Wong, H. and Iwai, H., On the scaling issues and high-κ replacement of ultrathin gate dielectrics for nanoscale MOS transistors, *Microelect. Eng.* **83**, 1867-1904 (2006).
11. Frerking, M. A. and Beauchamp, P. M., JPL Technology Readiness Assessment Guideline, *Aerosp Conf Proc*, 1-10 (2016).
12. Gonçalves Sotelo, G. *et al.*, A review of superconducting fault current limiters compared with other proven technologies, *Superconductivity* **3**, 100018 (2022).

13. Wilson, N. P., Yao, W., Shan, J., and Xu, X., Excitons and emergent quantum phenomena in stacked 2D semiconductors, *Nature* **599**, 383-392 (2021).
14. Qiu, D. Y., da Jornada, F. H., and Louie, S. G., Optical Spectrum ofMoS_2: Many-Body Effects and Diversity of Exciton States, *Phys. Rev. Lett.* **111**, 216805 (2013).
15. Ye, Z. *et al.*, Probing excitonic dark states in single-layer tungsten disulphide, *Nature* **513**, 214-218 (2014).
16. Komsa, H.-P. and Krasheninnikov, A. V., Effects of confinement and environment on the electronic structure and exciton binding energy of MoS_2 from first principles, *Phys. Rev. B* **86**, 241201(R) (2012).
17. Shimazaki, Y. *et al.*, Strongly correlated electrons and hybrid excitons in a moiré heterostructure, *Nature* **580**, 472-477 (2020).
18. Qi, R. *et al.*, Thermodynamic behavior of correlated electron-hole fluids in van der Waals heterostructures, *Nat. Commun.* **14**, 8264 (2023).
19. Weber, B. *et al.*, 2024 roadmap on 2D topological insulators, *J. Phys.: Mater.* **7**, 022501 (2024).
20. Zhang, H. *et al.*, Topological insulators in Bi_2Se_3, Bi_2Te_3 and Sb_2Te_3 with a single Dirac cone on the surface, *Nat. Phys.* **5**, 438-442 (2009).
21. Xia, Y. *et al.*, Observation of a large-gap topological-insulator class with a single Dirac cone on the surface, *Nat. Phys.* **5**, 398-402 (2009).
22. Moore, J. E., The birth of topological insulators, *Nature* **464**, 194-198 (2010).
23. Gong, C. and Zhang, X., Two-dimensional magnetic crystals and emergent heterostructure devices, *Science* **363**, 706 (2019).
24. Swamynadhan, M. J. and Ghosh, S., Designing multifunctional two-dimensional layered transition metal phosphorous chalcogenides, *Phys. Rev. Mater.* **5**, 054409 (2021).
25. Cysne, T. P. *et al.*, Orbital magnetoelectric effect in nanoribbons of transition metal dichalcogenides, *Phys. Rev. B* **107**, 115402 (2023).
26. Cardenas-Chirivi, G. *et al.*, Room temperature multiferroicity in a transition metal dichalcogenide, *npj 2D Mater. Appl.* **7**, 54 (2023).
27. Mak, K. F., Lee, C., Hone, J., Shan, J., and Heinz, T. F., Atomically Thin MoS_2: A New Direct-Gap Semiconductor, *Phys. Rev. Lett.* **105**, 136805 (2010).
28. Splendiani, A. *et al.*, Emerging Photoluminescence in Monolayer MoS_2, *Nano Lett.* **10**, 1271-1275 (2010).
29. Wang, Q. H., Kalantar-Zadeh, K., Kis, A., Coleman, J. N., and Strano, M. S., Electronics and optoelectronics of two-dimensional transition metal dichalcogenides, *Nat. Nanotech.* **7**, 699-712 (2012).
30. Sangwan, V. K. and Hersam, M. C., Electronic Transport in Two-Dimensional Materials, *Annu. Rev. of Phys. Chem.* **69**, 299-325 (2018).
31. Novoselov, K. S. *et al.*, Electric Field Effect in Atomically Thin Carbon Films, *Science* **306**, 666-669 (2004).
32. Wang, Q.-Y. *et al.*, Interface-Induced High-Temperature Superconductivity in Single Unit-Cell FeSe Films on $SrTiO_3$, *Chin. Phys. Lett.* **29**, 037402 (2012).
33. Lee, J. J. *et al.*, Interfacial mode coupling as the origin of the enhancement of T_c in FeSe films on $SrTiO_3$, *Nature* **515**, 245-248 (2014).
34. Moore, R. G. *et al.*, Monolayer Superconductivity and Tunable Topological Electronic Structure at the Fe(Te,Se)/Bi_2Te_3 Interface, *Adv. Mater.* **35**, 2210940 (2023).
35. Ugeda, M. M. *et al.*, Characterization of collective ground states in single-layer $NbSe_2$, *Nat. Phys.* **12**, 92-97 (2015).

36. Song, T. *et al.*, Unconventional superconducting quantum criticality in monolayer WTe_2, *Nat. Phys.* **20**, 269-274 (2024).
37. O'Hara, D. J. *et al.*, Room Temperature Intrinsic Ferromagnetism in Epitaxial Manganese Selenide Films in the Monolayer Limit, *Nano Lett.* **18**, 3125-3131 (2018).
38. Yu, W. *et al.*, Chemically Exfoliated VSe_2 Monolayers with Room-Temperature Ferromagnetism, *Adv. Mater.* **31**, 1903779 (2019).
39. Zhang, X. *et al.*, Room-temperature intrinsic ferromagnetism in epitaxial $CrTe_2$ ultrathin films, *Nat. Commun.* **12**, 2492 (2021).
40. Guan, S., Liu, C., Lu, Y., Yao, Y., and Yang, S. A., Tunable ferroelectricity and anisotropic electric transport in monolayer β-GeSe, *Phys. Rev. B* **97**, 144104 (2018).
41. Chang, K. *et al.*, Microscopic Manipulation of Ferroelectric Domains in SnSe Monolayers at Room Temperature, *Nano Lett.* **20**, 6590-6597 (2020).
42. Gao, W. and Chelikowsky, J. R., Prediction of Intrinsic Ferroelectricity and Large Piezoelectricity in Monolayer Arsenic Chalcogenides, *Nano Lett.* **20**, 8346-8352 (2020).
43. Higashitarumizu, N. *et al.*, Purely in-plane ferroelectricity in monolayer SnS at room temperature, *Nat. Commun.* **11**, 2428 (2020).
44. Guo, Y.-D. *et al.*, Sliding ferroelectricity in kagome-B_2X_3 (X = S, Se, Te) bilayers, *Appl. Phys. Lett.* **124**, 152901 (2024).
45. Wang, Q. *et al.*, Magnetic and Multiferroic Properties of Two-Dimensional $FePX_3$ and $CuFeP_2X_6$ (X = S, Se, and Te), *ACS Appl. Electron. Mater.* **7**, 660-666 (2025).
46. Yue, X. *et al.*, Single-layer MoSeN – a synthetic Janus two-dimensional transition-metal compound grown by plasma-assisted molecular beam epitaxy, *2D Mater.* **12**, 025004 (2025).
47. Wang, C., You, L., Cobden, D., and Wang, J., Towards two-dimensional van der Waals ferroelectrics, *Nat. Mater.* **22**, 542-552 (2023).
48. Zhang, D., Schoenherr, P., Sharma, P., and Seidel, J., Ferroelectric order in van der Waals layered materials, *Nat. Rev. Mater.* **8**, 25-40 (2022).
49. Gish, J. T., Lebedev, D., Song, T. W., Sangwan, V. K., and Hersam, M. C., Van der Waals opto-spintronics, *Nat. Electron.* **7**, 336-347 (2024).
50. Podzorov, V., Gershenson, M. E., Kloc, C., Zeis, R., and Bucher, E., High-mobility field-effect transistors based on transition metal dichalcogenides, *Appl. Phys. Lett.* **84**, 3301-3303 (2004).
51. Mitzi, D. B., Copel, M., and Chey, S. J., Low-Voltage Transistor Employing a High-Mobility Spin-Coated Chalcogenide Semiconductor, *Adv. Mater.* **17**, 1285-1289 (2005).
52. Mitzi, D. B., Copel, M., and Murray, C. E., High-Mobility p-Type Transistor Based on a Spin-Coated Metal Telluride Semiconductor, *Adv. Mater.* **18**, 2448-2452 (2006).
53. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V., and Kis, A., Single-layer MoS_2 transistors, *Nat. Nanotech.* **6**, 147-150 (2011).
54. Kim, S. *et al.*, High-mobility and low-power thin-film transistors based on multilayer MoS_2 crystals, *Nat. Commun.* **3**, 1038 (2012).
55. Cheng, R. *et al.*, Few-layer molybdenum disulfide transistors and circuits for high-speed flexible electronics, *Nat. Commun.* **5**, 1038 (2014).
56. Jadwiszczak, J. *et al.*, Mixed-Dimensional 1D/2D van der Waals Heterojunction Diodes and Transistors in the Atomic Limit, *ACS Nano* **16**, 1639-1648 (2022).
57. Yu, Y. *et al.*, Gate-tunable phase transitions in thin flakes of 1T-TaS_2, *Nat. Nanotech.* **10**, 270-276 (2015).
58. Li, H. M. *et al.*, Metal-semiconductor barrier modulation for high photoresponse in transition metal dichalcogenide field effect transistors, *Sci. Rep.* **4**, 4041 (2014).
59. Wang, H. *et al.*, Ultrafast Non-Volatile Floating-Gate Memory Based on All-2D Materials, *Adv. Mater.* **36**, e2311652 (2024).

60. Yang, H. *et al.*, Two-dimensional materials prospects for non-volatile spintronic memories, *Nature* **606**, 663-673 (2022).
61. Gwon, O. H. *et al.*, Systematic Design and Demonstration of Multi-Bit Generation in Layered Materials Heterostructures Floating-Gate Memory, *Adv. Funct. Mater.* **31**, 2105472 (2021).
62. Li, D. *et al.*, Two-dimensional non-volatile programmable p–n junctions, *Nat. Nanotech.* **12**, 901-906 (2017).
63. Sup Choi, M. *et al.*, Controlled charge trapping by molybdenum disulphide and graphene in ultrathin heterostructured memory devices, *Nat. Commun.* **4**, 1624 (2013).
64. Bertolazzi, S., Krasnozhon, D., and Kis, A., Nonvolatile memory cells based on MoS_2/graphene heterostructures, *ACS Nano* **7**, 3246-3252 (2013).
65. Joo, Y., Hwang, E., Hong, H., Cho, S., and Yang, H., Memory and Synaptic Devices Based on Emerging 2D Ferroelectricity, *Adv. Electron. Mater.* **9**, 2300211 (2023).
66. Liu, L. *et al.*, Ultrafast non-volatile flash memory based on van der Waals heterostructures, *Nat. Nanotech.* **16**, 874-881 (2021).
67. Zhang, B., Lu, P., Tabrizian, R., Feng, P. X. L., and Wu, Y., 2D Magnetic heterostructures: spintronics and quantum future, *npj Spintronics* **2**, 6 (2024).
68. Xie, Z. *et al.*, Orbital-selective spin texture and its manipulation in a topological insulator, *Nat. Commun.* **5**, 3382 (2014).
69. Rao, Z. *et al.*, Braiding reflectionless states in non-Hermitian magnonics, *Nat. Phys.* **20**, 1904-1911 (2024).
70. Chumak, A. V., Vasyuchka, V. I., Serga, A. A., and Hillebrands, B., Magnon spintronics, *Nat. Phys.* **11**, 453-461 (2015).
71. Jo, D., Go, D., Choi, G.-M., and Lee, H.-W., Spintronics meets orbitronics: Emergence of orbital angular momentum in solids, *npj Spintronics* **2**, 19 (2024).
72. Kajale, S. N., Hanna, J., Jang, K., and Sarkar, D., Two-dimensional magnetic materials for spintronic applications, *Nano Res.* **17**, 743-762 (2024).
73. Lin, X., Yang, W., Wang, K. L., and Zhao, W., Two-dimensional spintronics for low-power electronics, *Nat. Electron.* **2**, 274-283 (2019).
74. Suzuki, R. *et al.*, Valley-dependent spin polarization in bulk MoS_2 with broken inversion symmetry, *Nat. Nanotech.* **9**, 611-617 (2014).
75. Xiao, D., Liu, G.-B., Feng, W., Xu, X., and Yao, W., Coupled Spin and Valley Physics in Monolayers of MoS_2 and Other Group-VI Dichalcogenides, *Phys. Rev. Lett.* **108**, 196802 (2012).
76. Yakout, S. M., Spintronics: Future Technology for New Data Storage and Communication Devices, *J. Supercond. Nov. Magn.* **33**, 2557-2580 (2020).
77. Dieny, B. *et al.*, Opportunities and challenges for spintronics in the microelectronics industry, *Nat. Electron.* **3**, 446-459 (2020).
78. Avsar, A. *et al.*, Colloquium: Spintronics in graphene and other two-dimensional materials, *Rev. Mod. Phys.* **92**, 021003 (2020).
79. Ciarrocchi, A., Tagarelli, F., Avsar, A., and Kis, A., Excitonic devices with van der Waals heterostructures: valleytronics meets twistronics, *Nat. Rev. Mater.* **7**, 449-464 (2022).
80. Mak, K. F., He, K., Shan, J., and Heinz, T. F., Control of valley polarization in monolayer MoS_2 by optical helicity, *Nat. Nanotech.* **7**, 494-498 (2012).
81. Kumar, N., He, J., He, D., Wang, Y., and Zhao, H., Valley and spin dynamics in $MoSe_2$ two-dimensional crystals, *Nanoscale* **6**, 12690-12695 (2014).
82. Zeng, H., Dai, J., Yao, W., Xiao, D., and Cui, X., Valley polarization in MoS_2 monolayers by optical pumping, *Nat. Nanotech.* **7**, 490-493 (2012).
83. Cao, T. *et al.*, Valley-selective circular dichroism of monolayer molybdenum disulphide, *Nat. Commun.* **3**, 1038 (2012).

84. Lau, C. S. *et al.*, Dielectrics for Two-Dimensional Transition-Metal Dichalcogenide Applications, *ACS Nano* **17**, 9870-9905 (2023).
85. Vitale, S. A. *et al.*, Valleytronics: Opportunities, Challenges, and Paths Forward, *Small* **14**, 1801483 (2018).
86. Bussolotti, F. *et al.*, Roadmap on finding chiral valleys: screening 2D materials for valleytronics, *Nano Futures* **2**, 032001 (2018).
87. Ang, Y. S., Yang, S. A., Zhang, C., Ma, Z., and Ang, L. K., Valleytronics in merging Dirac cones: All-electric-controlled valley filter, valve, and universal reversible logic gate, *Phys. Rev. B* **96**, 245410 (2017).
88. Schaibley, J. R. *et al.*, Valleytronics in 2D materials, *Nat. Rev. Mater.* **1**, 16055 (2016).
89. Mak, K. F. and Shan, J., Photonics and optoelectronics of 2D semiconductor transition metal dichalcogenides, *Nat. Photon.* **10**, 216-226 (2016).
90. Liu, X. and Hersam, M. C., 2D materials for quantum information science, *Nat. Rev. Mater.* **4**, 669-684 (2019).
91. Xue, H., Yang, Y., and Zhang, B., Topological Valley Photonics: Physics and Device Applications, *Adv. Photonics Res.* **2** (2021).
92. Dong, Z. *et al.*, Broadband Excitonic Near-Infrared Photoresponse at the van der Waals Heterostructure/Metal Interface, *ACS Photonics* **11**, 4209 (2024).
93. Anantharaman, S. B. *et al.*, Ultrastrong light–matter coupling in two-dimensional metal–organic chalcogenolates, *Nat. Photon.* (2025).
94. Pham, P. V. *et al.*, 2D Heterostructures for Ubiquitous Electronics and Optoelectronics: Principles, Opportunities, and Challenges, *Chem. Rev.* **122**, 6514-6613 (2022).
95. Ponraj, J. S. *et al.*, Photonics and optoelectronics of two-dimensional materials beyond graphene, *Nanotechnology* **27**, 462001 (2016).
96. Molina-Sánchez, A., Hummer, K., and Wirtz, L., Vibrational and optical properties of MoS_2: From monolayer to bulk, *Surf. Sci. Rep.* **70**, 554-586 (2015).
97. Peng, B., Ang, P. K., and Loh, K. P., Two-dimensional dichalcogenides for light-harvesting applications, *Nano Today* **10**, 128-137 (2015).
98. Zhou, J. *et al.*, Probing plexciton emission from 2D materials on gold nanotrenches, *Nat. Commun.* **15**, 9583 (2024).
99. Saini, S. K. *et al.*, Unveiling Electric Bias Effects on Ultrafast Carrier Dynamics in Multiple Stacked ZnTe/Bi_2Te_3 Heterostructures, *J. Phys. Chem. C* **128**, 11687-11698 (2024).
100. Pospischil, A. and Mueller, T., Optoelectronic Devices Based on Atomically Thin Transition Metal Dichalcogenides, *Appl. Sci.* **6**, 78 (2016).
101. Rani, A., Verma, A., and Yadav, B. C., Advancements in transition metal dichalcogenides (TMDCs) for self-powered photodetectors: challenges, properties, and functionalization strategies, *Mater. Adv.* **5**, 3535-3562 (2024).
102. Lee, H. S. *et al.*, MoS_2 Nanosheet Phototransistors with Thickness-Modulated Optical Energy Gap, *Nano Lett.* **12**, 3695-3700 (2012).
103. Lopez-Sanchez, O., Lembke, D., Kayci, M., Radenovic, A., and Kis, A., Ultrasensitive photodetectors based on monolayer MoS_2, *Nat. Nanotech.* **8**, 497-501 (2013).
104. Yu, W. J. *et al.*, Highly efficient gate-tunable photocurrent generation in vertical heterostructures of layered materials, *Nat. Nanotech.* **8**, 952-958 (2013).
105. Velusamy, D. B. *et al.*, Flexible transition metal dichalcogenide nanosheets for band-selective photodetection, *Nat. Commun.* **6**, 1038 (2015).
106. Yan, F. *et al.*, Toward High-Performance Photodetectors Based on 2D Materials: Strategy on Methods, *Small Methods* **2**, 1700349 (2018).

107. Zatko, V. *et al.*, Band-Gap Landscape Engineering in Large-Scale 2D Semiconductor van der Waals Heterostructures, *ACS Nano* **15**, 7279-7289 (2021).
108. Huang, L. *et al.*, Enhanced light–matter interaction in two-dimensional transition metal dichalcogenides, *Rep. Prog. Phys.* **85**, 046401 (2022).
109. Chen, R. *et al.*, Monolayers of Germanene/Janus Ga_2SeTe van der Waals Heterostructures by First-Principles Calculations for High-Performance Optoelectronic Devices, *ACS Appl. Nano Mater.* **6**, 3453-3462 (2023).
110. Liao, L., Kovalska, E., Regner, J., Song, Q., and Sofer, Z., Two-Dimensional Van Der Waals Thin Film and Device, *Small* **20**, 2303638 (2023).
111. Wen, Y. and Wu, Z., High-performance photodetectors based on band alignment of type-I Te/WSe_2 and type-III Te/ReS_2 van der Waals heterostructures, *Chem. Phys. Lett.* **831**, 140849 (2023).
112. Tang, J. *et al.*, A Reliable All-2D Materials Artificial Synapse for High Energy-Efficient Neuromorphic Computing, *Adv. Funct. Mater.* **31**, 2011083 (2021).
113. Hadke, S., Kang, M. A., Sangwan, V. K., and Hersam, M. C., Two-Dimensional Materials for Brain-Inspired Computing Hardware, *Chem. Rev.* **125**, 835-932 (2025).
114. Liu, K. *et al.*, An optoelectronic synapse based on α-$In2Se_3$ with controllable temporal dynamics for multimode and multiscale reservoir computing, *Nat. Electron.* **5**, 761-773 (2022).
115. Zhai, Y. *et al.*, Reconfigurable 2D-ferroelectric platform for neuromorphic computing, *Appl. Phys. Rev.* **10**, 011408 (2023).
116. Sangwan, V. K., Liu, S. E., Trivedi, A. R., and Hersam, M. C., Two-dimensional materials for bio-realistic neuronal computing networks, *Matter* **5**, 4133-4152 (2022).
117. Yan, X., Qian, J. H., Sangwan, V. K., and Hersam, M. C., Progress and Challenges for Memtransistors in Neuromorphic Circuits and Systems, *Adv. Mater.* **34**, 2108025 (2022).
118. Sangwan, V. K. and Hersam, M. C., Neuromorphic nanoelectronic materials, *Nat. Nanotech.* **15**, 517-528 (2020).
119. Gupta, S. *et al.*, Low Power, CMOS-MoS_2 Memtransistor based Neuromorphic Hybrid Architecture for Wake-Up Systems, *Sci. Rep.* **9**, 15604 (2019).
120. Soliman, M. *et al.*, Photoferroelectric All-van-der-Waals Heterostructure for Multimode Neuromorphic Ferroelectric Transistors, *ACS Appl. Mater. Interfaces* **15**, 15732-15744 (2023).
121. Zhang, Z. *et al.*, 2D materials and van der Waals heterojunctions for neuromorphic computing, *Neuromorph. Comp. Eng.* **2**, 032004 (2022).
122. Ai, L. *et al.*, Van der Waals ferromagnetic Josephson junctions, *Nat. Commun.* **12**, 2650 (2021).
123. Banerjee, A., Sundaresh, A., Ganesan, R., and Kumar, P. S. A., Signatures of Topological Superconductivity in Bulk-Insulating Topological Insulator $BiSbTe_{1.25}Se_{1.75}$ in Proximity with Superconducting $NbSe_2$, *ACS Nano* **12**, 12665-12672 (2018).
124. Chen, W. *et al.*, Temperature Effects on the Electronic Structures of Epitaxial 1T'-WSe_2 Monolayers, *J. Phys. Chem. Lett.* **16**, 2188-2195 (2025).
125. Fu, L. and Kane, C. L., Superconducting proximity effect and majorana fermions at the surface of a topological insulator, *Phys. Rev. Lett.* **100**, 096407 (2008).
126. Li, Y. W. *et al.*, Observation of topological superconductivity in a stoichiometric transition metal dichalcogenide 2M-WS_2, *Nat. Commun.* **12**, 2874 (2021).
127. Mong, R. S. K. *et al.*, Universal Topological Quantum Computation from a Superconductor-Abelian Quantum Hall Heterostructure, *Phys. Rev. X* **4**, 011036 (2014).
128. Nayak, C., Simon, S. H., Stern, A., Freedman, M., and Das Sarma, S., Non-Abelian anyons and topological quantum computation, *Rev. Mod. Phys.* **80**, 1083-1159 (2008).
129. Ren, H. *et al.*, Topological superconductivity in a phase-controlled Josephson junction, *Nature* **569**, 93-98 (2019).

130. Sarma, S. D., Freedman, M., and Nayak, C., Majorana zero modes and topological quantum computation, *npj Quant. Info.* **1**, 15001 (2015).
131. Xu, J.-P. *et al.*, Artificial Topological Superconductor by the Proximity Effect, *Phys. Rev. Lett.* **112**, 217001 (2014).
132. Yuan, Y. *et al.*, Evidence of anisotropic Majorana bound states in 2M-WS_2, *Nat. Phys.* **15**, 1046-1051 (2019).
133. Kitaev, A. Y., Fault-tolerant quantum computation by anyons, *Ann. Phys.* **303**, 2-30 (2003).
134. Manzeli, S., Ovchinnikov, D., Pasquier, D., Yazyev, O. V., and Kis, A., 2D transition metal dichalcogenides, *Nat. Rev. Mater.* **2**, 17033 (2017).
135. Liu, C. *et al.*, Two-dimensional materials for next-generation computing technologies, *Nat. Nanotechnol.* **15**, 545-557 (2020).
136. Allain, A., Kang, J., Banerjee, K., and Kis, A., Electrical contacts to two-dimensional semiconductors, *Nat. Mater.* **14**, 1195-1205 (2015).
137. Xia, F., Perebeinos, V., Lin, Y. M., Wu, Y., and Avouris, P., The origins and limits of metal-graphene junction resistance, *Nat. Nanotechnol.* **6**, 179-184 (2011).
138. Qiu, H. *et al.*, Hopping transport through defect-induced localized states in molybdenum disulphide, *Nat. Commun.* **4**, 2642 (2013).
139. Liu, Y. *et al.*, Van der Waals heterostructures and devices, *Nat. Rev. Mater.* **1**, 16042 (2016).
140. Das, S., Chen, H. Y., Penumatcha, A. V., and Appenzeller, J., High performance multilayer MoS_2 transistors with scandium contacts, *Nano Lett.* **13**, 100-105 (2013).
141. Cui, X. *et al.*, Multi-terminal transport measurements of MoS_2 using a van der Waals heterostructure device platform, *Nat. Nanotechnol.* **10**, 534-540 (2015).
142. Hong, J. *et al.*, Exploring atomic defects in molybdenum disulphide monolayers, *Nat. Commun.* **6**, 6293 (2015).
143. Ly, T. H., Zhao, J., Cichocka, M. O., Li, L. J., and Lee, Y. H., Dynamical observations on the crack tip zone and stress corrosion of two-dimensional MoS_2, *Nat. Commun.* **8**, 14116 (2017).
144. Giubileo, F. and Di Bartolomeo, A., The role of contact resistance in graphene field-effect devices, *Prog. Surf. Sci.* **92**, 143-175 (2017).
145. Yang, Q. *et al.*, Constrained patterning of orientated metal chalcogenide nanowires and their growth mechanism, *Nat. Commun.* **15**, 6074 (2024).
146. Liu, Y. *et al.*, Toward barrier free contact to molybdenum disulfide using graphene electrodes, *Nano Lett.* **15**, 3030-3034 (2015).
147. Jiang, J., Xu, T., Lu, J., Sun, L., and Ni, Z., Defect Engineering in 2D Materials: Precise Manipulation and Improved Functionalities, *Research* **2019**, 4641739 (2019).
148. Lee, C. H. *et al.*, Atomically thin p-n junctions with van der Waals heterointerfaces, *Nat. Nanotechnol.* **9**, 676-681 (2014).
149. Choi, K., Lee, Y. T., and Im, S., Two-dimensional van der Waals nanosheet devices for future electronics and photonics, *Nano Today* **11**, 626-643 (2016).
150. Novoselov, K. S., Mishchenko, A., Carvalho, A., and Castro Neto, A. H., 2D materials and van der Waals heterostructures, *Science* **353**, aac9439 (2016).
151. Zhang, X. *et al.*, Van der Waals-Interface-Dominated All-2D Electronics, *Adv. Mater.* **35**, e2207966 (2023).
152. Geim, A. K. and Grigorieva, I. V., Van der Waals heterostructures, *Nature* **499**, 419-425 (2013).
153. Zhou, W. *et al.*, Intrinsic structural defects in monolayer molybdenum disulfide, *Nano Lett.* **13**, 2615-2622 (2013).
154. Li, M. *et al.*, Imperfection-enabled memristive switching in van der Waals materials, *Nat. Electron.* **6**, 491-505 (2023).

155. Mitterreiter, E. *et al.*, Atomistic Positioning of Defects in Helium Ion Treated Single-Layer MoS_2, *Nano Lett.* **20**, 4437-4444 (2020).
156. Chua, R. *et al.*, Can Reconstructed Se-Deficient Line Defects in Monolayer VSe_2 Induce Magnetism?, *Adv. Mater.* **32**, e2000693 (2020).
157. Karni, O. *et al.*, Infrared Interlayer Exciton Emission in MoS_2/WSe_2 Heterostructures, *Phys. Rev. Lett.* **123**, 247402 (2019).
158. He, Z. *et al.*, Defect Engineering in Single-Layer MoS_2 Using Heavy Ion Irradiation, *ACS Appl. Mater. Interfaces.* **10**, 42524-42533 (2018).
159. Lu, J. *et al.*, Atomic healing of defects in transition metal dichalcogenides, *Nano Lett.* **15**, 3524-3532 (2015).
160. Cho, S. *et al.*, DEVICE TECHNOLOGY. Phase patterning for ohmic homojunction contact in $MoTe_2$, *Science* **349**, 625-628 (2015).
161. Lembke, D. and Kis, A., Breakdown of high-performance monolayer MoS_2 transistors, *ACS Nano* **6**, 10070-10075 (2012).
162. Baugher, B. W., Churchill, H. O., Yang, Y., and Jarillo-Herrero, P., Intrinsic electronic transport properties of high-quality monolayer and bilayer MoS_2, *Nano Lett.* **13**, 4212-4216 (2013).
163. Kim, M. *et al.*, 2D Materials in the Display Industry: Status and Prospects, *Adv. Mater.* **35**, e2205520 (2023).
164. Li, S. *et al.*, Enhanced Electrical Performance of Monolayer MoS_2 with Rare Earth Element Sm Doping, *Nanomaterials* **11** (2021).
165. Mir, S. H., Yadav, V. K., and Singh, J. K., Recent Advances in the Carrier Mobility of Two-Dimensional Materials: A Theoretical Perspective, *ACS Omega* **5**, 14203-14211 (2020).
166. Liu, H., Neal, A. T., and Ye, P. D., Channel length scaling of MoS_2 MOSFETs, *ACS Nano* **6**, 8563-8569 (2012).
167. Jariwala, D., Sangwan, V. K., Lauhon, L. J., Marks, T. J., and Hersam, M. C., Emerging device applications for semiconducting two-dimensional transition metal dichalcogenides, *ACS Nano* **8**, 1102-1120 (2014).
168. Das, S. *et al.*, Transistors based on two-dimensional materials for future integrated circuits, *Nat. Electron.* **4**, 786-799 (2021).
169. Chhowalla, M. *et al.*, The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets, *Nat. Chem.* **5**, 263-275 (2013).
170. Fang, H. *et al.*, High-performance single layered WSe_2 p-FETs with chemically doped contacts, *Nano Lett.* **12**, 3788-3792 (2012).
171. Chen, Y. *et al.*, Tunable band gap photoluminescence from atomically thin transition-metal dichalcogenide alloys, *ACS Nano* **7**, 4610-4616 (2013).
172. Kang, J., Tongay, S., Zhou, J., Li, J., and Wu, J., Band offsets and heterostructures of two-dimensional semiconductors, *Applied Physics Letters* **102** (2013).
173. Sundaram, R. S. *et al.*, Electroluminescence in single layer MoS_2, *Nano Lett.* **13**, 1416-1421 (2013).
174. Mann, J. *et al.*, 2-dimensional transition metal dichalcogenides with tunable direct band gaps: $MoS_{2(1-x)}Se_{2x}$ monolayers, *Adv. Mater.* **26**, 1399-1404 (2014).
175. Kang, M. *et al.*, Universal Mechanism of Band-Gap Engineering in Transition-Metal Dichalcogenides, *Nano Lett.* **17**, 1610-1615 (2017).
176. Zeng, L. H. *et al.*, Fast, Self-Driven, Air-Stable, and Broadband Photodetector Based on Vertically Aligned $PtSe_2$/GaAs Heterojunction, *Adv. Funct. Mater.* **28** (2018).
177. Radisavljevic, B. and Kis, A., Mobility engineering and a metal-insulator transition in monolayer MoS_2, *Nat. Mater.* **12**, 815-820 (2013).

178. Yoon, Y., Ganapathi, K., and Salahuddin, S., How good can monolayer MoS_2 transistors be?, *Nano Lett.* **11**, 3768-3773 (2011).
179. Liu, H., Gu, J., and Ye, P. D., MoS_2 Nanoribbon Transistors: Transition From Depletion Mode to Enhancement Mode by Channel-Width Trimming, *IEEE Electron Device Letters* **33**, 1273-1275 (2012).
180. Radisavljevic, B., Whitwick, M. B., and Kis, A., Integrated circuits and logic operations based on single-layer MoS_2, *ACS Nano* **5**, 9934-9938 (2011).
181. Jaikissoon, M. *et al.*, CMOS-compatible strain engineering for monolayer semiconductor transistors, *Nat. Electron.* **7**, 885-891 (2024).
182. Lembke, D., Bertolazzi, S., and Kis, A., Single-layer MoS_2 electronics, *Acc. Chem. Res.* **48**, 100-110 (2015).
183. Xhameni, A. *et al.*, Forming and compliance-free operation of low-energy, fast-switching HfO_xS_y/HfS_2 memristors, *Nanoscale Horiz.* **10**, 616-627 (2025).
184. Yang, Q. *et al.*, Controlled Optoelectronic Response in van der Waals Heterostructures for In-Sensor Computing, *Adv. Funct. Mater.* **32**, 2207290 (2022).
185. Deng, Y. *et al.*, Large-area growth of synaptic heterostructure arrays for integrated neuromorphic visual perception chips, *Chip* **3**, 100088 (2024).
186. Tang, B. *et al.*, Solution-processable 2D materials for monolithic 3D memory-sensing-computing platforms: opportunities and challenges, *npj 2D Mater. Appl.* **8**, 74 (2024).
187. Chen, C., Zhou, Y., Tong, L., Pang, Y., and Xu, J., Emerging 2D Ferroelectric Devices for In-Sensor and In-Memory Computing, *Adv. Mater.* **37**, e2400332 (2025).
188. Yang, P. *et al.*, Epitaxial Growth of Centimeter-Scale Single-Crystal MoS_2 Monolayer on Au(111), *ACS Nano* **14**, 5036-5045 (2020).
189. Choi, J. H. *et al.*, A Strategy for Wafer-Scale Crystalline MoS_2 Thin Films with Controlled Morphology Using Pulsed Metal–Organic Chemical Vapor Deposition at Low Temperature, *Adv. Mater. Interfaces* **9**, 2101785 (2021).
190. Hong, W., Park, C., Shim, G. W., Yang, S. Y., and Choi, S. Y., Wafer-Scale Uniform Growth of an Atomically Thin MoS_2 Film with Controlled Layer Numbers by Metal-Organic Chemical Vapor Deposition, *ACS Appl. Mater. Interfaces* **13**, 50497-50504 (2021).
191. Qin, B. *et al.*, General low-temperature growth of two-dimensional nanosheets from layered and nonlayered materials, *Nat. Commun.* **14**, 304 (2023).
192. Pinto, F. M. *et al.*, Recent Advances in Layered MX_2-Based Materials (M = Mo, W and X = S, Se, Te) for Emerging Optoelectronic and Photo(electro)catalytic Applications, *Catalysts* **14**, 388 (2024).
193. Kim, S. Y., Kwak, J., Ciobanu, C. V., and Kwon, S. Y., Recent Developments in Controlled Vapor-Phase Growth of 2D Group 6 Transition Metal Dichalcogenides, *Adv. Mater.* **31**, e1804939 (2019).
194. Choudhury, T. H., Zhang, X., Al Balushi, Z. Y., Chubarov, M., and Redwing, J. M., Epitaxial Growth of Two-Dimensional Layered Transition Metal Dichalcogenides, *Ann. Rev. Mater. Res.* **50**, 155-177 (2020).
195. Liang, Q., Zhang, Q., Zhao, X., Liu, M., and Wee, A. T. S., Defect Engineering of Two-Dimensional Transition-Metal Dichalcogenides: Applications, Challenges, and Opportunities, *ACS Nano* **15**, 2165-2181 (2021).
196. Turchanin, A. and George, A., Tailored Growth of Transition Metal Dichalcogenides' Monolayers by Chemical Vapor Deposition, *Small*, e2403089 (2024).
197. Xue, G. *et al.*, Large-Area Epitaxial Growth of Transition Metal Dichalcogenides, *Chem. Rev.* **124**, 9785-9865 (2024).

198. Kroemer, H., Nobel Lecture: Quasielectric fields and band offsets: teaching electrons new tricks, *Rev. Mod. Phys.* **73**, 783-793 (2001).
199. Freund, L. B., The mechanics of electronic materials, *Int. J. of Solids Struct.* **37**, 185-196 (2000).
200. Bickel, J. E., Modine, N. A., Van der Ven, A., and Mirecki Millunchick, J., Atomic size mismatch strain induced surface reconstructions, *Appl. Phys. Lett.* **92**, 062104 (2008).
201. Giantomassi, M. *et al.*, Electronic properties of interfaces and defects from many-body perturbation theory: Recent developments and applications, *Phys. Status Solidi B* **248**, 275-289 (2011).
202. Dong, J. *et al.*, Transmission electron microscopy of epitaxial semiconductor materials and devices, *J. Phys. D: Appl. Phys.* **58**, 043001 (2024).
203. Yao, X. *et al.*, Hybrid Symmetry Epitaxy of the Superconducting Fe(Te,Se) Film on a Topological Insulator, *Nano Lett.* **21**, 6518-6524 (2021).
204. Yao, X. *et al.*, Superconducting Fourfold Fe(Te,Se) Film on Sixfold Magnetic MnTe via Hybrid Symmetry Epitaxy, *Nano Lett.* **22**, 7522-7526 (2022).
205. Chen, A. H. *et al.*, Interfacially Enhanced Superconductivity in Fe(Te,Se)/Bi_4Te_3 Heterostructures, *Adv. Mater.* **36**, e2401809 (2024).
206. Yi, H. *et al.*, Crossover from Ising- to Rashba-type superconductivity in epitaxial Bi_2Se_3/monolayer $NbSe_2$ heterostructures, *Nat. Mater.* **21**, 1366-1372 (2022).
207. Zhu, D. *et al.*, Highly efficient charge-to-spin conversion from in situ Bi_2Se_3/Fe heterostructures, *Appl. Phys. Lett.* **118**, 062403 (2021).
208. MacNeill, D. *et al.*, Control of spin–orbit torques through crystal symmetry in WTe_2/ferromagnet bilayers, *Nat. Phys.* **13**, 300-305 (2016).
209. Furchi, M. M., Pospischil, A., Libisch, F., Burgdorfer, J., and Mueller, T., Photovoltaic effect in an electrically tunable van der Waals heterojunction, *Nano Lett.* **14**, 4785-4791 (2014).
210. He, J., Hummer, K., and Franchini, C., Stacking effects on the electronic and optical properties of bilayer transition metal dichalcogenides MoS_2, $MoSe_2$, WS_2, and WSe_2, *Phys. Rev. B* **89**, 075409 (2014).
211. Liu, K. *et al.*, Evolution of interlayer coupling in twisted molybdenum disulfide bilayers, *Nat. Commun.* **5**, 4966 (2014).
212. Xia, F., Wang, H., Xiao, D., Dubey, M., and Ramasubramaniam, A., Two-dimensional material nanophotonics, *Nat. Photon.* **8**, 899-907 (2014).
213. Seyler, K. L. *et al.*, Electrical control of second-harmonic generation in a WSe_2 monolayer transistor, *Nat. Nanotechnol.* **10**, 407-411 (2015).
214. Amani, M. *et al.*, Solution-Synthesized High-Mobility Tellurium Nanoflakes for Short-Wave Infrared Photodetectors, *ACS Nano* **12**, 7253-7263 (2018).
215. Trovatello, C. *et al.*, The ultrafast onset of exciton formation in 2D semiconductors, *Nat. Commun.* **11**, 5277 (2020).
216. Regan, E. C. *et al.*, Emerging exciton physics in transition metal dichalcogenide heterobilayers, *Nat. Rev. Mater.* **7**, 778-795 (2022).
217. Hichri, A., Amara, I. B., Ayari, S., and Jaziri, S., Dielectric environment and/or random disorder effects on free, charged and localized excitonic states in monolayer WS_2, *J. Phys. Condens. Matter.* **29**, 435305 (2017).
218. Van der Donck, M. and Peeters, F. M., Interlayer excitons in transition metal dichalcogenide heterostructures, *Phys. Rev. B* **98**, 115104 (2018).
219. Pei, J., Yang, J., Yildirim, T., Zhang, H., and Lu, Y., Many-Body Complexes in 2D Semiconductors, *Adv. Mater.* **31**, e1706945 (2019).

220. Waldecker, L. *et al.*, Rigid Band Shifts in Two-Dimensional Semiconductors through External Dielectric Screening, *Phys. Rev. Lett.* **123**, 206403 (2019).
221. Moore, D. *et al.*, Uncovering topographically hidden features in 2D $MoSe_2$ with correlated potential and optical nanoprobes, *npj 2D Mater. Appl.* **4**, 44 (2020).
222. Ji, J. and Choi, J. H., Understanding the Effects of Dielectric Property, Separation Distance, and Band Alignment on Interlayer Excitons in 2D Hybrid MoS_2/WSe_2 Heterostructures, *ACS Appl. Electron. Mater.* **3**, 3052-3059 (2021).
223. Maserati, L. *et al.*, Anisotropic 2D excitons unveiled in organic-inorganic quantum wells, *Mater. Horiz.* **8**, 197-208 (2021).
224. Kitaev, A., Anyons in an exactly solved model and beyond, *Ann. Phys.* **321**, 2-111 (2006).
225. Rebec, S. N. *et al.*, Coexistence of Replica Bands and Superconductivity in FeSe Monolayer Films, *Phys. Rev. Lett.* **118**, 067002 (2017).
226. Li, J. *et al.*, Intrinsic magnetic topological insulators in van der Waals layered $MnBi_2Te_4$-family materials, *Sci. Adv.* **5**, eaaw5685 (2019).
227. Liu, C. *et al.*, Robust axion insulator and Chern insulator phases in a two-dimensional antiferromagnetic topological insulator, *Nat. Mater.* **19**, 522-527 (2020).
228. Sekine, A. and Nomura, K., Axion electrodynamics in topological materials, *J. Appl. Phys.* **129**, 141101 (2021).
229. Yang, S. *et al.*, Odd-Even Layer-Number Effect and Layer-Dependent Magnetic Phase Diagrams in $MnBi_2Te_4$, *Phys. Rev. X* **11**, 011003 (2021).
230. Chen, B. *et al.*, Even-Odd Layer-Dependent Exchange Bias Effect in $MnBi_2Te_4$ Chern Insulator Devices, *Nano Lett.* **24**, 8320-8326 (2024).
231. Li, Y. *et al.*, Fabrication-induced even-odd discrepancy of magnetotransport in few-layer $MnBi_2Te_4$, *Nat. Commun.* **15**, 3399 (2024).
232. Walsh, L. A. *et al.*, Interface Chemistry of Contact Metals and Ferromagnets on the Topological Insulator Bi_2Se_3, *J. Phys. Chem. C* **121**, 23551-23563 (2017).
233. Bonell, F. *et al.*, Control of Spin-Orbit Torques by Interface Engineering in Topological Insulator Heterostructures, *Nano Lett.* **20**, 5893-5899 (2020).
234. Kappera, R. *et al.*, Phase-engineered low-resistance contacts for ultrathin MoS_2 transistors, *Nat. Mater.* **13**, 1128-1134 (2014).
235. Wang, H. *et al.*, Theoretical and Experimental Investigation on 3d Transition Metal Anisotropic Diffusion in van Der Waals Layered Sb_2Te_3, *J. Phys. Chem. C* **128**, 6859-6867 (2024).
236. Liu, X. *et al.*, On-device phase engineering, *Nat. Mater.* **23**, 1363-1369 (2024).
237. Bai, M. *et al.*, Proximity-induced superconductivity in $(Bi_{1-x}Sb_x)_2Te_3$ topological-insulator nanowires, *Commun. Mater.* **3**, 20 (2022).
238. Wei, X. K. *et al.*, Atomic Diffusion-Induced Polarization and Superconductivity in Topological Insulator-Based Heterostructures, *ACS Nano* **18**, 571-580 (2024).
239. Zhu, W. *et al.*, Electronic transport and device prospects of monolayer molybdenum disulphide grown by chemical vapour deposition, *Nat. Commun.* **5**, 3087 (2014).
240. Jariwala, D. *et al.*, Band-like transport in high mobility unencapsulated single-layer MoS_2 transistors, *Appl. Phys. Lett.* **102**, 173107 (2013).
241. Li, S. L. *et al.*, Thickness-dependent interfacial Coulomb scattering in atomically thin field-effect transistors, *Nano Lett.* **13**, 3546-3552 (2013).
242. Li, S. L., Tsukagoshi, K., Orgiu, E., and Samori, P., Charge transport and mobility engineering in two-dimensional transition metal chalcogenide semiconductors, *Chem. Soc. Rev.* **45**, 118-151 (2016).
243. Jia, T. *et al.*, Epitaxial growth of $TiSe_2/TiO_2$ heterostructure, *2D Mater.* **6**, 011008 (2018).

244. Liu, H. and Ye, P. D., Atomic-layer-deposited Al_2O_3 on Bi_2Te_3 for topological insulator field-effect transistors, *App. Phys. Lett.* **99**, 052108 (2011).
245. Lang, M. *et al.*, Revelation of Topological Surface States in Bi_2Se_3 Thin Films by In Situ Al Passivation, *ACS Nano* **6**, 295-302 (2012).
246. Cho, A.-J. and Kwon, J.-Y., Hexagonal Boron Nitride for Surface Passivation of Two-Dimensional van der Waals Heterojunction Solar Cells, *ACS Appl. Mater. Interfaces* **11**, 39765-39771 (2019).
247. You, Y. G. *et al.*, Atomic layer deposited Al_2O_3 passivation layer for few-layer WS_2 field effect transistors, *Nanotechnology* **32**, 505702 (2021).
248. See Supplemental Information at (web link to be added) for a practical guide to nanofabrication issues and potential solutions.
249. Yun, H. *et al.*, Removal of photoresist residues and healing of defects on graphene using H_2 and CH_4 plasma, *Appl. Surf. Sci.* **463**, 802-808 (2019).
250. Liang, J. *et al.*, Impact of Post-Lithography Polymer Residue on the Electrical Characteristics of MoS_2 and WSe_2 Field Effect Transistors, *Adv. Mater. Interfaces* **6**, 1801321 (2018).
251. Deng, C. *et al.*, Reversible Charge-Transfer Doping in Graphene due to Reaction with Polymer Residues, *J. Phys. Chem. C* **118**, 13890-13897 (2014).
252. Ono, Y. and Im, H., Thermal annealing effects on graphene/n-Si Schottky junction solar cell: removal of PMMA residues, *Jpn. J. Appl. Phys.* **62**, 045002 (2023).
253. Kim, Y. D. *et al.*, Bright visible light emission from graphene, *Nat. Nanotechnol.* **10**, 676-681 (2015).
254. Wang, X. *et al.*, Direct Observation of Poly(Methyl Methacrylate) Removal from a Graphene Surface, *Chem. Mater.* **29**, 2033-2039 (2017).
255. Vishwanath, S. *et al.*, Controllable growth of layered selenide and telluride heterostructures and superlattices using molecular beam epitaxy, *J. Mater. Res.* **31**, 900-910 (2016).
256. Guo, Y., Zhou, S., and Zhao, J., Oxidation Behaviors of Two-dimensional Metal Chalcogenides, *Chem. Nano. Mat.* **6**, 838-849 (2020).
257. Joseph, T. *et al.*, Nonstoichiometric Phases of Two-Dimensional Transition-Metal Dichalcogenides: From Chalcogen Vacancies to Pure Metal Membranes, *J. Phys. Chem. Lett.* **10**, 6492-6498 (2019).
258. Lehtinen, O. *et al.*, Atomic scale microstructure and properties of Se-deficient two-dimensional $MoSe_2$, *ACS Nano* **9**, 3274-3283 (2015).
259. Blades, W. H., Frady, N. J., Litwin, P. M., McDonnell, S. J., and Reinke, P., Thermally Induced Defects on WSe_2, *J. Phys. Chem. C* **124**, 15337-15346 (2020).
260. Peng, Q. *et al.*, Local laser heating effects in monolayer WS_2 probed by photoluminescence, *Appl. Surf. Sci.* **562**, 150226 (2021).
261. Chow, P. K. *et al.*, Defect-induced photoluminescence in monolayer semiconducting transition metal dichalcogenides, *ACS Nano* **9**, 1520-1527 (2015).
262. Mitterreiter, E. *et al.*, The role of chalcogen vacancies for atomic defect emission in MoS_2, *Nat. Commun.* **12**, 3822 (2021).
263. Tian, W., Yu, W., Shi, J., and Wang, Y., The Property, Preparation and Application of Topological Insulators: A Review, *Materials* **10**, 814 (2017).
264. Scanlon, D. O. *et al.*, Controlling bulk conductivity in topological insulators: key role of anti-site defects, *Adv. Mater.* **24**, 2154-2158 (2012).
265. Amigó, M. L. *et al.*, Intrinsic pinning by naturally occurring correlated defects in $FeSe_{1-x}Te_x$ superconductors, *Supercond. Sci. Tech.* **30**, 085010 (2017).

266. Liu, Y., Xing, Q., Dennis, K. W., McCallum, R. W., and Lograsso, T. A., Evolution of precipitate morphology during heat treatment and its implications for the superconductivity in $K_xFe_{1.6+y}Se_2$ single crystals, *Phys. Rev. B* **86**, 144507 (2012).
267. Ahn, Y., Kim, H., Kim, Y.-H., Yi, Y., and Kim, S.-I., Procedure of removing polymer residues and its influences on electronic and structural characteristics of graphene, *Appl. Phys. Lett.* **102**, 091602 (2013).
268. Xue, J. *et al.*, Scanning tunnelling microscopy and spectroscopy of ultra-flat graphene on hexagonal boron nitride, *Nat. Mater.* **10**, 282-285 (2011).
269. Lapano, J. *et al.*, van der Waals Epitaxy Growth of Bi_2Se_3 on a Freestanding Monolayer Graphene Membrane: Implications for Layered Materials and Heterostructures, *ACS Appl. Nano Mater.* **4**, 7607-7613 (2021).
270. Matsumae, T., Koehler, A. D., Suga, T., and Hobart, K. D., A Scalable Clean Graphene Transfer Process Using Polymethylglutarimide as a Support Scaffold, *J. Electrochem. Soc.* **163**, E159-E161 (2016).
271. Lin, Y. C. *et al.*, Graphene annealing: how clean can it be?, *Nano Lett.* **12**, 414-419 (2012).
272. Liu, M. *et al.*, Temperature-Triggered Sulfur Vacancy Evolution in Monolayer MoS_2/Graphene Heterostructures, *Small* **13** (2017).
273. Li, L. *et al.*, Role of Sulfur Vacancies and Undercoordinated Mo Regions in MoS_2 Nanosheets toward the Evolution of Hydrogen, *ACS Nano* **13**, 6824-6834 (2019).
274. Jung, M.-H. and Choi, H.-S., Photoresist etching using Ar/O_2 and He/O_2 atmospheric pressure plasma, *Thin Solid Films* **515**, 2295-2302 (2006).
275. Harada, K., Plasma etching durability of poly(methyl methacrylate), *J. Appl. Poly. Sci.* **26**, 1961-1973 (2003).
276. Zhang, C., Yang, C., and Ding, D., Deep reactive ion etching of PMMA, *Appl. Surf. Sci.* **227**, 139-143 (2004).
277. Sikora, A. *et al.*, Surface modification of PMMA polymer and its composites with $PC_{61}BM$ fullerene derivative using an atmospheric pressure microwave argon plasma sheet, *Sci. Rep.* **11**, 9270 (2021).
278. Mohammed, N. Q. and Murbat, H. H., Polymethyl methacrylate (PMMA) surface treatment by DBD cold atmospheric plasma in air, *AIP Conf. Proc.* **3036**, 050022 (2024).
279. Le, Q. T. *et al.*, Removal of post-etch photoresist and sidewall residues using organic solvent and additive combined with physical forces, *Microelect. Eng.* **86**, 181-185 (2009).
280. Dabral, A., Lu, A. K. A., Chiappe, D., Houssa, M., and Pourtois, G., A systematic study of various 2D materials in the light of defect formation and oxidation, *Phys. Chem. Chem. Phys.* **21**, 1089-1099 (2019).
281. Jalilian, R. *et al.*, Scanning gate microscopy on graphene: charge inhomogeneity and extrinsic doping, *Nanotechnology* **22**, 295705 (2011).
282. Son, B. H. *et al.*, Electron beam induced removal of PMMA layer used for graphene transfer, *Sci. Rep.* **7**, 18058 (2017).
283. Hwang, H. J., Lee, Y., Cho, C., and Lee, B. H., Facile process to clean PMMA residue on graphene using KrF laser annealing, *AIP Advances* **8**, 105326 (2018).
284. Bolotin, K. I. *et al.*, Ultrahigh electron mobility in suspended graphene, *Solid State Commun.* **146**, 351-355 (2008).
285. Du, X., Skachko, I., Barker, A., and Andrei, E. Y., Approaching ballistic transport in suspended graphene, *Nat. Nanotechnol.* **3**, 491-495 (2008).
286. Burns, D. W., in *MEMS Materials and Processes Handbook*, edited by R. Ghodssi, and P. Lin (Springer US, Boston, MA, 2011), pp. 457-665.

287. Mogi, M. *et al.*, Experimental signature of the parity anomaly in a semi-magnetic topological insulator, *Nat. Phys.* **18**, 390-394 (2022).
288. Yang, F. *et al.*, Dual-gated topological insulator thin-film device for efficient Fermi-level tuning, *ACS Nano* **9**, 4050-4055 (2015).
289. Legg, H. F. *et al.*, Giant magnetochiral anisotropy from quantum-confined surface states of topological insulator nanowires, *Nat. Nanotechnol.* **17**, 696-700 (2022).
290. Rossler, M. *et al.*, Top-Down Fabrication of Bulk-Insulating Topological Insulator Nanowires for Quantum Devices, *Nano. Lett.* **23**, 2846-2853 (2023).
291. Ma, E. Y. *et al.*, Unexpected edge conduction in mercury telluride quantum wells under broken time-reversal symmetry, *Nat. Commun.* **6**, 7252 (2015).
292. Maier, H. *et al.*, Ballistic geometric resistance resonances in a single surface of a topological insulator, *Nat. Commun.* **8**, 2023 (2017).
293. Li, M. *et al.*, From Top to Down—Recent Advances in Etching of 2D Materials, *Adv. Mater. Interfaces* **9**, 2201334 (2022).
294. Muranaka, S. *et al.*, Anisotropic Wet Etching of WSe_2 and MoS_2 for Twist-Angle Extraction of Heterobilayers, *J. Phys. Chem. C* **128**, 7211-7215 (2024).
295. Munkhbat, B. *et al.*, Transition metal dichalcogenide metamaterials with atomic precision, *Nat. Commun.* **11**, 4604 (2020).
296. Yasuda, K. *et al.*, Nonreciprocal charge transport at topological insulator/superconductor interface, *Nat. Commun.* **10**, 2734 (2019).
297. Danielsen, D. R. *et al.*, Super-Resolution Nanolithography of Two-Dimensional Materials by Anisotropic Etching, *ACS Appl. Mater. Interfaces* **13**, 41886-41894 (2021).
298. Zhu, T. *et al.*, Electrostatic modulation of thermoelectric transport properties of 2H-$MoTe_2$, *Energy Advances* **2**, 1882-1892 (2023).
299. Sha, Y., Xiao, S., Zhang, X., Qin, F., and Gu, X., Layer-by-layer thinning of $MoSe_2$ by soft and reactive plasma etching, *Appl. Surf. Sci.* **411**, 182-188 (2017).
300. Xiao, S. *et al.*, Atomic-layer soft plasma etching of MoS_2, *Sci. Rep.* **6**, 19945 (2016).
301. Li, P. *et al.*, Evidence for topological type-II Weyl semimetal WTe_2, *Nat. Commun.* **8**, 2150 (2017).
302. Huff, M., Recent Advances in Reactive Ion Etching and Applications of High-Aspect-Ratio Microfabrication, *Micromachines* **12**, 991 (2021).
303. Karouta, F., A practical approach to reactive ion etching, *J. Phys. D* **47**, 233501 (2014).
304. He, T. *et al.*, Etching Techniques in 2D Materials, *Adv. Mater. Tech.* **4**, 1900064 (2019).
305. Barton, A. T. *et al.*, Impact of Etch Processes on the Chemistry and Surface States of the Topological Insulator Bi_2Se_3, *ACS Appl. Mater. Interfaces* **11**, 32144-32150 (2019).
306. Li, J. *et al.*, Direct evidence of reactive ion etching induced damages in $Ge_2Sb_2Te_5$ based on different halogen plasmas, *Appl. Surf. Sci.* **378**, 163-166 (2016).
307. Kim, K. S. *et al.*, Atomic Layer Etching Mechanism of MoS_2 for Nanodevices, *ACS Appl. Mater. Interfaces* **9**, 11967-11976 (2017).
308. Nipane, A. *et al.*, Damage-Free Atomic Layer Etch of WSe_2: A Platform for Fabricating Clean Two-Dimensional Devices, *ACS Appl. Mater. Interfaces* **13**, 1930-1942 (2021).
309. Lin, T. *et al.*, Controlled Layer-by-Layer Etching of MoS_2, *ACS Appl. Mater. Interfaces* **7**, 15892-15897 (2015).
310. Tsai, Y., Li, Z., and Hu, S., Recent Progress of Atomic Layer Technology in Spintronics: Mechanism, Materials and Prospects, *Nanomaterials* **12**, 661 (2022).
311. Höflich, K. *et al.*, Roadmap for focused ion beam technologies, *Appl. Phys. Rev.* **10**, 041311 (2023).

312. Ziegler, J. F., Ziegler, M. D., and Biersack, J. P., SRIM – The stopping and range of ions in matter (2010), *Nuclear Inst. Methods Phys. Res. B* **268**, 1818-1823 (2010).
313. Thiruraman, J. P., Masih Das, P., and Drndić, M., Irradiation of Transition Metal Dichalcogenides Using a Focused Ion Beam: Controlled Single-Atom Defect Creation, *Adv. Funct. Mater.* **29**, 1904668 (2019).
314. Telkhozhayeva, M. and Girshevitz, O., Roadmap toward Controlled Ion Beam-Induced Defects in 2D Materials, *Adv. Funct. Mater.* **34**, 2404615 (2024).
315. Sarcan, F. *et al.*, Understanding the impact of heavy ions and tailoring the optical properties of large-area monolayer WS_2 using focused ion beam, *npj 2D Mater. Appl.* **7**, 23 (2023).
316. Friedensen, S., Mlack, J. T., and Drndic, M., Materials analysis and focused ion beam nanofabrication of topological insulator Bi_2Se_3, *Sci. Rep.* **7**, 13466 (2017).
317. Gracia-Abad, R., Sangiao, S., Kumar Chaluvadi, S., Orgiani, P., and Teresa, J. M., Ion-Induced Lateral Damage in the Focused Ion Beam Patterning of Topological Insulator Bi_2Se_3 Thin Films, *Materials* **16**, 2244 (2023).
318. Liu, J. *et al.*, Effect of Ion Irradiation Introduced by Focused Ion-Beam Milling on the Mechanical Behaviour of Sub-Micron-Sized Samples, *Sci. Rep.* **10**, 10324 (2020).
319. Burnell, G. *et al.*, Planar superconductor-normal-superconductor Josephson junctions in MgB_2, *Appl. Phys. Lett.* **79**, 3464-3466 (2001).
320. Bell, C. *et al.*, Fabrication of nanoscale heterostructure devices with a focused ion beam microscope, *Nanotechnology* **14**, 630-632 (2003).
321. Burnell, G. *et al.*, Directly coupled superconducting quantum interference device magnetometer fabricated in magnesium diboride by focused ion beam, *Appl. Phys. Lett.* **81**, 102-104 (2002).
322. Brinkman, A. *et al.*, Superconducting quantum interference device based on MgB_2 nanobridges, *Appl. Phys. Lett.* **79**, 2420-2422 (2001).
323. Cybart, S. A. *et al.*, Nano Josephson superconducting tunnel junctions in $YBa_2Cu_3O_{7-\delta}$ directly patterned with a focused helium ion beam, *Nat. Nanotechnol.* **10**, 598-602 (2015).
324. Müller, B. *et al.*, Josephson Junctions and SQUIDs Created by Focused Helium-Ion-Beam Irradiation of $YBa_2Cu_3O_7$, *Phys. Rev. Applied* **11**, 044082 (2019).
325. Kennedy, O. W. *et al.*, Tunable Nb Superconducting Resonator Based on a Constriction Nano-SQUID Fabricated with a Ne Focused Ion Beam, *Phys. Rev. Applied* **11**, 014006 (2019).
326. Urbanek, M. *et al.*, Focused ion beam fabrication of spintronic nanostructures: an optimization of the milling process, *Nanotechnology* **21**, 145304 (2010).
327. Kang, S. *et al.*, Highly enhanced ferroelectricity in HfO_2-based ferroelectric thin film by light ion bombardment, *Science* **376**, 731-738 (2022).
328. Klein, J. *et al.*, Site-selectively generated photon emitters in monolayer MoS_2 via local helium ion irradiation, *Nat. Commun.* **10**, 2755 (2019).
329. Janoch, R., Gabor, A. M., Anselmo, A., and Dubé, C. E., Contact Resistance Measurement - Observations on Technique and Test Parameters, *Ieee Phot Spec Conf*, 1-6 (2015).
330. Muñoz-Rojo, M., Caballero-Calero, O., and Martín-González, M., Electrical contact resistances of thermoelectric thin films measured by Kelvin probe microscopy, *Appl. Phys. Lett.* **103**, 183905 (2013).
331. Duflou, R., Pourtois, G., Houssa, M., and Afzalian, A., Fundamentals of low-resistive 2D-semiconductor metal contacts: an ab-initio NEGF study, *npj 2D Mater. Appl.* **7**, 38 (2023).
332. Wang, Y. *et al.*, Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors, *Nature* **568**, 70-74 (2019).
333. Farmanbar, M. and Brocks, G., Controlling the Schottky barrier at MoS_2/metal contacts by inserting a BN monolayer, *Phys. Rev. B* **91**, 161304(R) (2015).

334. Nagareddy, V. K. *et al.*, High temperature measurements of metal contacts on epitaxial graphene, *Appl. Phys. Lett.* **99**, 073506 (2011).
335. Smith, J. T., Franklin, A. D., Farmer, D. B., and Dimitrakopoulos, C. D., Reducing contact resistance in graphene devices through contact area patterning, *ACS Nano* **7**, 3661-3667 (2013).
336. Kim, H. *et al.*, Selective Surface Passivation for Ultrathin and Continuous Metallic Films via Atomic Layer Deposition, *Nano Lett.* **25**, 4101-4107 (2025).
337. Ma, L., Wang, Y., and Liu, Y., van der Waals Contact for Two-Dimensional Transition Metal Dichalcogenides, *Chem. Rev.* **124**, 2583-2616 (2024).
338. Saifur Rahman, M., Agyapong, A. D., and Mohney, S. E., Effect of physical vapor deposition on contacts to 2D MoS_2, *J. Appl. Phys.* **136**, 224303 (2024).
339. Raub, C. J., Superconductivity of the platinum metals and their alloys, *Materials & Design* **5**, 129-136 (1984).
340. Bai, M. *et al.*, Novel self-epitaxy for inducing superconductivity in the topological insulator $(Bi_{1-x}Sb_x)_2Te_3$, *Phys. Rev. Mater.* **4**, 094801 (2020).
341. Rosen, I. T. *et al.*, Fractional AC Josephson effect in a topological insulator proximitized by a self-formed superconductor, *Phys. Rev. B* **110**, 064511 (2024).
342. Yun, H. *et al.*, Stencil nano lithography based on a nanoscale polymer shadow mask: towards organic nanoelectronics, *Sci. Rep.* **5**, 10220 (2015).
343. Nguyen, V. L. *et al.*, Wafer-scale integration of transition metal dichalcogenide field-effect transistors using adhesion lithography, *Nat. Electron.* **6**, 146-153 (2022).
344. Park, J. Y. *et al.*, Double-sided van der Waals epitaxy of topological insulators across an atomically thin membrane, *Nat. Mater.* **24**, 399-405 (2025).
345. Kwak, I. C. *et al.*, Orthogonal photopatterning of two-dimensional percolated network films for wafer-scale heterostructures, *Nat. Electron.* **8**, 235-243 (2025).
346. Andersen, M. P. *et al.*, Low-damage electron beam lithography for nanostructures on Bi_2Te_3-class topological insulator thin films, *J. Appl. Phys.* **133** (2023).
347. Migliato Marega, G. *et al.*, A large-scale integrated vector–matrix multiplication processor based on monolayer molybdenum disulfide memories, *Nat. Electron.* **6**, 991-998 (2023).
348. Li, H. *et al.*, Recent Experimental Breakthroughs on 2D Transistors: Approaching the Theoretical Limit, *Adv. Funct. Mater.* **34** (2024).
349. Schram, T., Sutar, S., Radu, I., and Asselberghs, I., Challenges of Wafer-Scale Integration of 2D Semiconductors for High-Performance Transistor Circuits, *Adv. Mater.* **34** (2022).

Figures

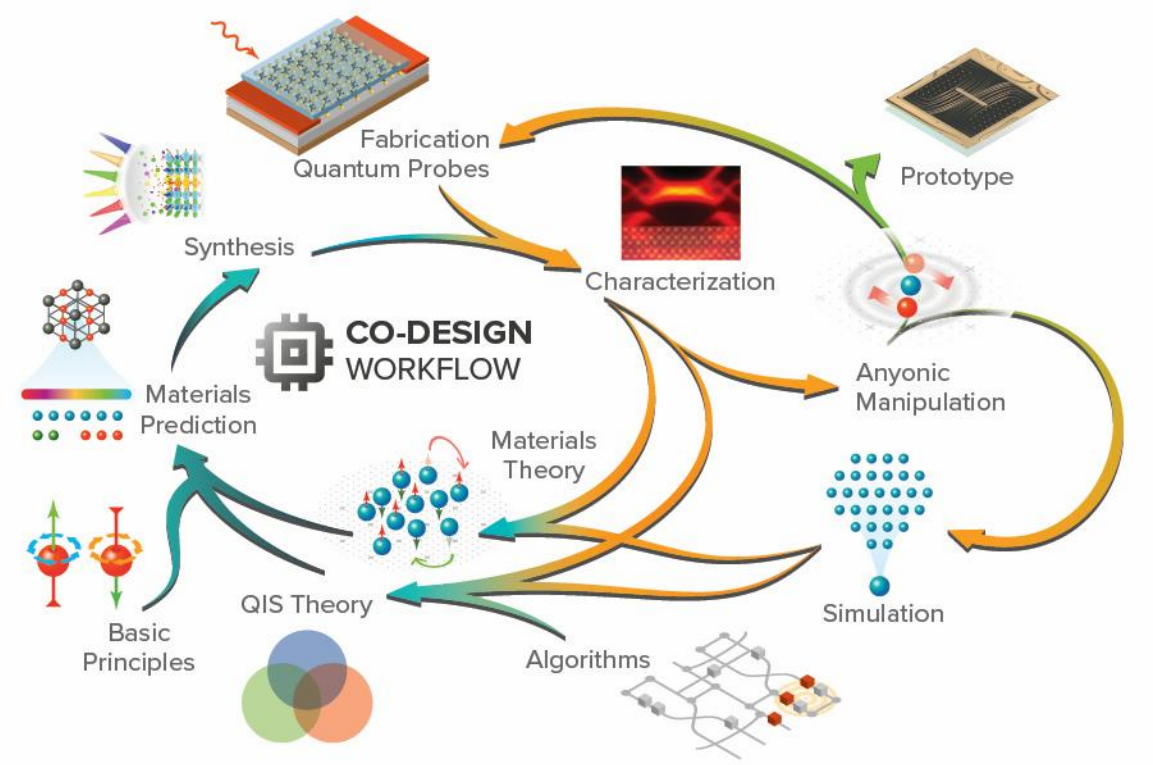

Fig. 1 | A conceptual co-design workflow for quantum technologies. The inherent sensitivity and coupling of quantum states preclude a simple linear trajectory from fundamental quantum principles to functional prototype devices. Material interfaces and fabrication-induced defects significantly affect device performance in the quantum realm, necessitating their careful integration at every stage of development.

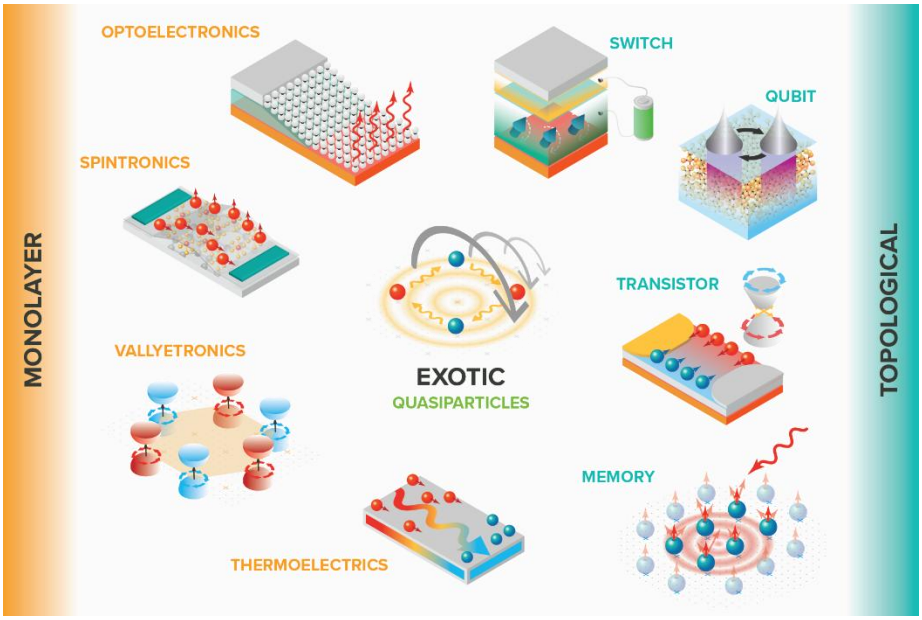

Fig. 2 | Chalcogenide materials host numerous exotic quasiparticles, including topologically protected states, opening pathways to numerous use-inspired applications. These advances have the potential to transform technology beyond conventional charge-based paradigms, thus moving beyond Moore's law. Realizing such applications requires the development of scalable device fabrication processes compatible with this class of materials.

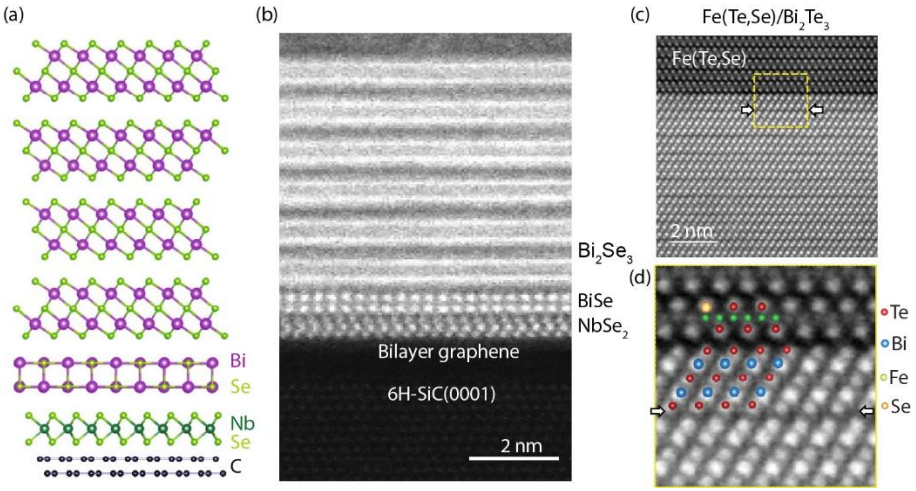

Fig. 3 | Interfacial structure. **a,b** Schematic and cross-sectional scanning transmission electron microscopy (STEM) image of Bi_2Se_3/monolayer $NbSe_2$ heterostructure on bilayer graphene. A BiSe interfacial layer is formed at the heterojunction. Reproduced, with permission of Springer Nature, from Ref. 206. **c,d** STEM images of Fe(Te,Se)/Bi_2Te_3 heterostructure. The schematic overlay in **d** highlights the epitaxial interface with no reconstruction. Reproduced, with permission of Wiley, from Ref. 205.

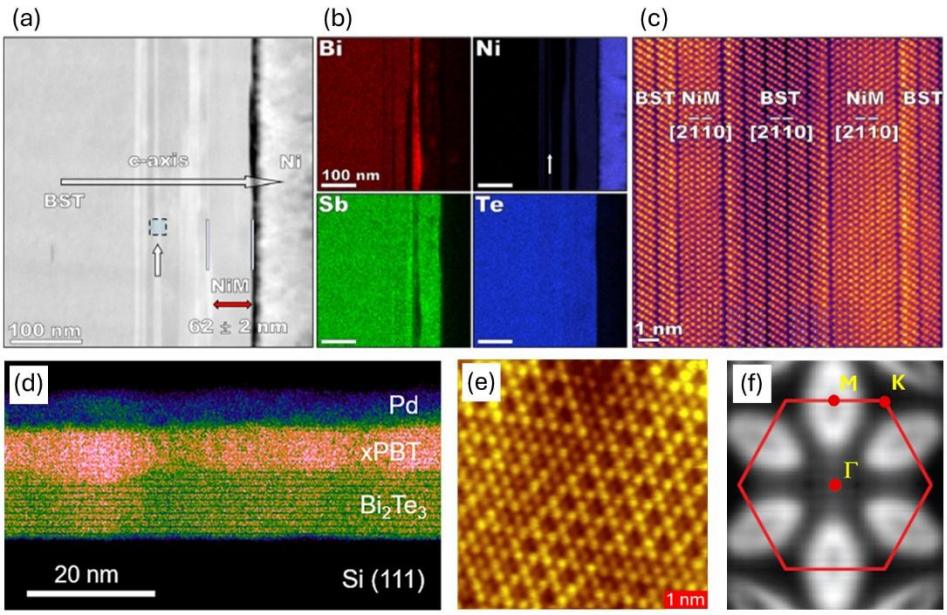

Fig. 4 | Cross-interface diffusion. **a** Low-magnification STEM image of $Bi_xSb_{2-x}Te_3$ (BST)/NiM/Ni interface where M denotes mixture of Bi, Sb, and Te. **b** Energy Dispersive Spectra (EDS) maps showing distribution of Bi, Sb, Te, and Ni at the interface. **c** Atomic-resolution STEM image of the interface for the dashed box in **a**. Reproduced, with permission of ACS, from Ref. 235. **d** Low-magnification STEM image of Pd/*x*PBT/Bi_2Te_3 heterostructure grown on a Si(111) substrate where *x*PBT is a Pd diffusion induced intermediate $Pd_{1+x}(Bi_{0.4}Te_{0.2})_2$ phase. Reproduced, with permission of ACS, from Ref. 238. Figure showing interlayer diffusion. **e,f** Synthesis of $TiSe_2$ on TiO_2 substrate by the diffusion of Ti. **e** Scanning Tunneling Microscopy (STM) image showing the surface atomic structure of $TiSe_2$. **f** The Fermi surface of $TiSe_2$ grown on TiO_2 as shown by Angle Resolved Photoemission Spectroscopy (ARPES). Reproduced, with permission of IOP, from Ref. 243. The $TiSe_2$ atomic and electronic structure is the same as cleaved bulk $TiSe_2$ crystals except for a shift of the Fermi level due to charge transfer between the film and the substrate.

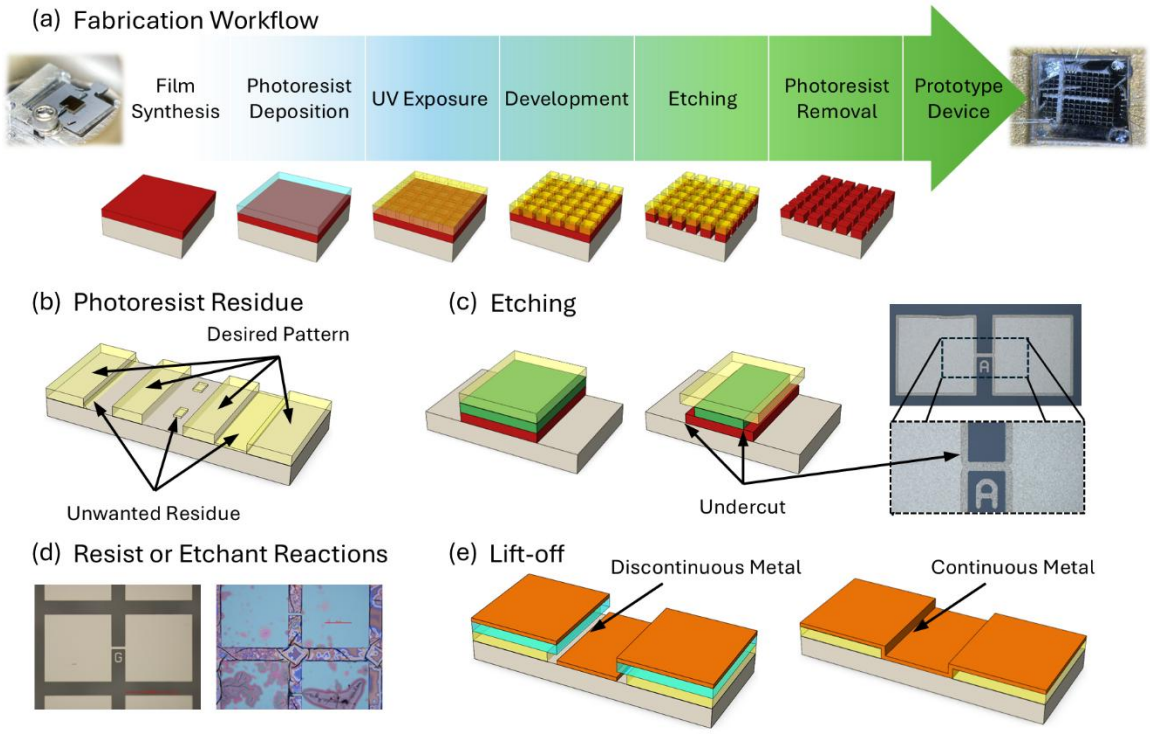

Fig. 5 | Device workflow and pitfalls. **a** Overview of the workflow from thin film to device prototype. **b** Schematic illustrating the post-lithography state, where thin layers of photoresist residue remain after development. **c** Schematics comparing dry etching (left) and wet etching (center). Wet etching produces an undercut, whose extent varies among different material layers. Scanning Electron Microscope (SEM) images (right) show an example where the color contrast is due to an undercut around the device edge. **d** SEM images of a successful (left) and an unsuccessful (right) prototype fabricated under near identical conditions. The hypersensitivity of chalcogenide materials demands careful processing to avoid unwanted chemical reactions. **e** Schematic of the lift-off process comparing two resist configurations: a bilayer (left) and a single-layer (right). In the bilayer configuration, differing development rates create an overhang that causes the metal layer to break at the top, enabling a cleaner lift-off. By contrast, a continuous metal film in the single-layer approach can inadvertently lift off with the resist, risking unwanted metal removal.

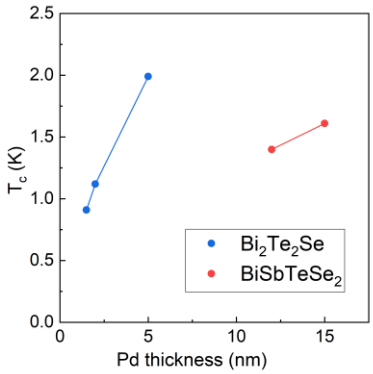

Fig. 6 | Variation of superconducting transition temperature with Pd overlayer thickness on Bi_2Te_2Se and $BiSbTeSe_2$.

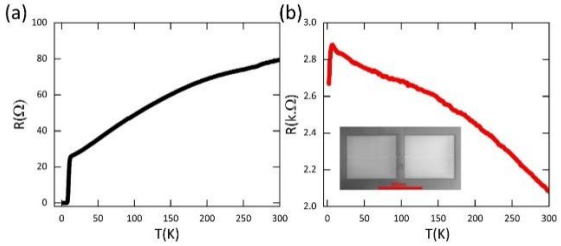

Fig. 7 | Resistance vs. temperature plot of as grown thin film (**a**) showing superconducting behavior and FIB patterned device (**b**) with Xe^+ ion beam revealing superconductivity has been destroyed. Inset: SEM image of the patterned device.

SUPPLEMENTARY INFORMATION: Next-Generation Electronics by Co-Design with Chalcogenide Materials

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Supplementary Table 1: Issues with Lithography for chalcogenides and possible solutions:

Issues with lithography for chalcogenides	Solutions
• Baking the resist (for photo- or electron beam lithography) may lead to the loss of chalcogen elements, which can subsequently impair the electrical properties of the material. This issue is notably significant for chalcogenide materials, as they are particularly susceptible to such degradation.	• For lithography on chalcogenide materials, it is advisable to avoid pre-baking or post-baking the resist, or to restrict the baking duration to lower temperatures (approximately 50-60°C). Without baking the resist, it will be necessary to re-optimize both the exposure time for photolithography and the exposure dose for electron beam lithography, as well as the development time, to achieve similar results as those obtained with baked resist. Generally, baking the resist before lithography tends to reduce the required exposure time/dose and development duration, thereby streamlining the process. Another solution could be the use of shadow masks as an alternate route to lithography, wherever possible[4–10].
• Resist residue can create significant challenges during subsequent stages, particularly during the lift-off process. This residue may lead to incomplete material removal, unpredictable surface properties, or contamination, ultimately compromising the quality and performance of the final device[1–3].	• This common issue can be addressed through several approaches: 1. mild oxygen plasma treatment, 2. wet cleaning, 3. contact atomic force microscopy (C-AFM), and 4. thermal treatment in a vacuum or inert atmosphere[11–13]. Among these methods, wet cleaning is often preferred for chalcogenide-based materials, as it does not involve any heating. C-AFM can also be effectively employed. However, caution is warranted with oxygen plasma ashing, which is widely used in both industry and research. It is essential to carefully control the plasma power and duration, as excessive exposure can lead to oxidation of the delicate chalcogenide 2D materials and/or oxygen can also diffuse from side, while attempting to remove resist residue.

Supplementary Table 2: Issues with Wet-Etching for chalcogenides and possible solutions:

Issues with Wet etching for chalcogenides	Solutions
• Isotropic etching with wet etchants can lead to undercutting, which may damage chalcogenide-based devices[14].	• This well-known challenge associated with wet etching can generally be minimized by selecting an appropriate etchant with a suitable etch rate—neither too fast nor too slow. For chalcogenide devices, an etching time of approximately 1 minute is typically effective. Another approach is to harden the mask[15]; for instance, post-baking the photoresist (such as AZ series) for less than a minute can enhance the rigidity of the resist and help reduce undercutting. However, it is crucial to carefully optimize both the temperature and duration of post-baking to avoid degrading the device while effectively addressing the undercutting issue. Additionally, employing a hard mask, such as Al_2O_3, can help mitigate undercutting, although this method requires an additional etching step to remove the hard mask afterward[16,17]. Argon/Xenon ion milling is a widely used technique known for its highly directional nature, which minimizes undesired isotopic etching. However, it can lead to an increase in sample temperature. To mitigate this thermal issue, strategies such as cooling the sample stage or conducting the milling in multiple steps can be effective. Ion milling serves as a viable alternative to traditional wet etching and reactive ion etching (RIE).
• Utilizing strong inorganic acids for etching chalcogenides can offer effective material removal; however, it is essential to consider the potential for damaging the underlying structure or altering the material properties.	• Strong acids such as HCl, HNO_3 and HBr are effective wet etchants for chalcogenides. However, using these acids in their concentrated form can lead to unacceptably high etch rates, resulting in excessive undercutting. Therefore, diluting the strong acids is necessary to achieve better control over the etching process. It is recommended to

	avoid using HF as it can attack the resist even at low concentration. Common diluents include H_2O, H_2O_2, and organic acids like acetic acid (CH_3COOH) and phosphoric acid (H_3PO_4)[18–25]. Mixing a strong acid with various diluting agents can enhance the etching of chalcogenides. The correct dilution ratio is critical, as over-dilution can slow down the etching process significantly. A typical starting ratio is 1 part acid to 10-30 parts diluting agent. However, there is no universal ratio applicable to all chalcogenide-based materials, so it's advisable to begin with the suggested ratio and adjust as necessary based on specific requirements and outcomes.
• Significantly reduced etch rate.	• This situation may occur when initially optimizing the etching recipe with strong acids and diluting agents. To enhance the etch rate, it is often beneficial to increase the temperature by several tens of degrees. Typically, a temperature increase of around 10 degrees Celsius can potentially double the etch rate. However, it is crucial to exercise caution, as excessively high temperatures may lead to thermal damage to the chalcogenides. Alternatively, slightly increasing the acid concentration can also help achieve a suitable etch rate without the risks associated with elevated temperatures.

Supplementary Table 3: Issues with Reactive-Ion-Etching (RIE) for chalcogenides and possible solutions:

Issues with RIE for chalcogenides	Solutions
• Introduction of defects, modification of stoichiometry, and alterations in electrical properties.	• This issue is particularly relevant for chalcogenide-based layered materials, as it can degrade their unique properties. The highly energetic ion beam can heat the sample stage sufficiently to cause the chalcogen material to lose its chalcogen elements[26–28]. Therefore, implementing effective cooling strategies for the sample stage is crucial when working with these materials. • Using low-energy plasma can help maintain a lower ambient temperature, although it may prolong the etching process and still risk heating the sample. Introducing argon into the chamber enables more efficient etching with reduced plasma power, as the heavier Ar^{++} ions can displace atoms through physical collisions, complementing the chemical reactions facilitated by fluorine or chlorine gas species (e.g., SF_6, CHF_3, Cl_2, BCl_3)[29,30]. A typical ratio of argon gas to fluorine/chlorine gas is 1:10. Importantly, the use of oxygen (O_2) alongside these gases is not recommended for chalcogenides, in contrast to other non-chalcogenide materials, such as graphene. • Another solution would be the use of Atomic layer etching (ALE) where layer by layer etching is enabled by the cyclic exposure to the precursors[31–33]. This field is still in development phase for the chalcogenides. The caution during the use of ALE for chalcogenide etching would be to reduce the ambient heating stage temperature to be as low as possible.
• Etching byproducts can deposit on the sidewalls of the etched regions, leading to alterations in the material's properties.	• For chalcogenide materials, typical byproducts include chalcogen-halides. These can be effectively removed using strong acids diluted to the appropriate concentrations, as previously discussed.

Supplementary Table 4: Issues with Electrical Contacts for chalcogenides and possible solutions:

Issues with electrical contacts for chalcogenides	Solutions
• High contact resistance[34]	• This is a well-recognized challenge in the development of functional devices based on chalcogenides. Possible solutions include: 1. Choice of Metals: Selecting the right metal can significantly reduce the work function difference with chalcogenides, thereby minimizing contact resistance (CR). Gold (Au) has demonstrated excellent performance as it forms Ohmic contacts with chalcogenide materials. However, Au suffers from poor adhesion to transition metal dichalcogenides (TMDs). To improve adhesion, alternative metals such as chromium (Cr), titanium (Ti), and palladium (Pd) can be used, with Ti being particularly effective[35,36]. Consequently, the Ti/Au combination has become a widely favored choice for contact metals in chalcogenide-based devices In/Au recently is gaining attention for having very low CR on 2d materials[37]. 2. Current Crowding: Current crowding occurs when there is a low contact area between the metal and the material. Implementing edge contacts has proven to be an effective strategy for mitigating this issue in layered chalcogenide-based materials[34,36]. 3. Mild Etching: Employing mild inert-gas plasma etching prior to metal deposition can be highly beneficial in reducing contact resistance[38–40]. It is crucial to keep plasma power and etching duration low while carefully optimizing these parameters to achieve the desired results.

• Damage to the thin layered sample during the deposition process.	• The most common techniques for metal deposition are sputtering and electron beam (e-beam) evaporation. During sputtering, the kinetic energy of the metal atoms is significantly higher—ranging from 10 to 100 times that of atoms deposited via e-beam evaporation—which can lead to damage to the thin layers of chalcogenides. The extent of this damage can also be influenced by other factors, such as deposition pressure and the distance between the sample and the metal targets. As a result, e-beam evaporation is generally preferred over sputtering for metal deposition on chalcogenide-based materials[41].

Supplementary Table 5: Issues with Lift-off for chalcogenides and possible solutions:

Issues with lift-off for chalcogenides	Solutions
• Incomplete lift-off of metal from the chalcogenide materials.	• This common issue arises from poor adhesion between the metal and the chalcogenide layer, often due to resist residue and other organic contaminants. To enhance the lift-off process, a gentle argon plasma cleaning for approximately 1 minute can significantly improve results. Additionally, using a warm N-methyl-2-pyrrolidone (NMP) solution at around 50°C has proven to be more effective for lift-off than acetone, particularly when working with chalcogenides.

Supplementary Table 6: Issues with Focused-Ion-Beam (FIB) for chalcogenides and possible solutions:

Issues with Focussed ion beam for chalcogenides	Solutions
• Introduces numerous defects and significantly alters the properties of chalcogenide-based materials[42].	• This issue is particularly relevant for chalcogenide-based layered materials, as their properties can change drastically when device sizes are reduced[43–45]. The damage can propagate laterally over considerable distances within the material. The potential solutions include: 1. Utilization of Low Beam Current and Low Beam Energy: Employing a low beam current of approximately 10 pA and moderate beam energy in the range of 5 kV can significantly reduce damage[46,47], although this approach may extend the etching time. One effective strategy is to start with higher beam energy (in the nA-μA range) and a higher beam current when the beam is focused away from the central region of the device, allowing for quicker etching. Once the beam is closer to the central channel, the beam energy and current can be lowered to the previously mentioned levels. 2. Use of a Hard Mask: Often, the tail of the focused ion beam can damage undesired areas of the chalcogenide sample. To mitigate this, a hard mask (such as Al_2O_3 or Si_3N_4) or simply resist can be patterned on top of the chalcogenide sample to serve as a protective shield against stray ion beams[42].
• The localized heat generated during irradiation can lead to damage in the chalcogenide film.	• The most effective way to mitigate the heating effect is to utilize low beam energy and low beam current, as described in the previous segment.

References:

1. Liang, J. et al. Impact of Post-Lithography Polymer Residue on the Electrical Characteristics of MoS_2 and WSe_2 Field Effect Transistors. *Adv. Mater. Interfaces* **6**, 1801321 (2019).

2. Deng, C. *et al.* Reversible Charge-Transfer Doping in Graphene due to Reaction with Polymer Residues. *J. Phys. Chem. C* **118**, 13890–13897 (2014).

3. Yun, H. *et al.* Removal of photoresist residues and healing of defects on graphene using H_2 and CH_4 plasma. *Appl. Surf. Sci.* **463**, 802–808 (2019).

4. Op het Veld, R. L. M. *et al.* In-plane selective area InSb–Al nanowire quantum networks. *Commun. Phys.* **3**, 1–7 (2020).

5. Lee, Joon Sue, et al. Selective-area chemical beam epitaxy of in-plane InAs one-dimensional channels grown on InP (001), InP (111) B, and InP (011) surfaces. *Phys. Rev. Mater.* **3**, 084606 (2019).

6. Mukherjee, Shagorika, et al. Shadow Mask Molecular Beam Epitaxy for In-Plane Gradient Permittivity Materials. *Adv. Funct. Mater.* **34**, 2411069 (2024).

7. Goswami, A. *et al.* Sn/InAs Josephson Junctions on Selective Area Grown Nanowires with in Situ Shadowed Superconductor Evaporation. *Nano Lett.* **23**, 7311–7318 (2023).

8. Schüffelgen, P. *et al.* Selective area growth and stencil lithography for in situ fabricated quantum devices. *Nat. Nanotechnol.* **14**, 825–831 (2019).

9. von den Driesch, N. *et al.* Shadow Wall Epitaxy of Compound Semiconductors toward All in Situ Fabrication of Quantum Devices. *ACS Appl. Electron. Mater.* **6**, 6246–6252 (2024).

10. Pendharkar, M., et al. Parity-preserving and magnetic field–resilient superconductivity in InSb nanowires with Sn shells. *Science* **372**, 508-511 (2021).

11. Ahn, Youngkun, et al. Procedure of removing polymer residues and its influences on electronic and structural characteristics of graphene. *Appl. Phys. Lett.* **102**, 9 (2013).

12. Jung, M.-H. & Choi, H.-S. Photoresist etching using Ar/O_2 and He/O_2 atmospheric pressure plasma. *Thin Solid Films* **515**, 2295–2302 (2006).

13. Le, Q. T. *et al.* Removal of post-etch photoresist and sidewall residues using organic solvent and additive combined with physical forces. *Microelectron. Eng.* **86**, 181–185 (2009).

14. Ghodssi, R. & Lin, P. *MEMS Materials and Processes Handbook*. (Springer Science & Business Media, 2011).

15. Madou, M. J. *Manufacturing Techniques for Microfabrication and Nanotechnology*. (CRC Press, 2011).

16. Bondareva, J. *et al*. Wet scandium etching for hard mask formation on a silicon substrate. *Thin Solid Films* **762**, 139543 (2022).

17. Tummala, R. R., Haley, M. R. & Czornyj, G. Materials in microelectronics. *Ceram. Int.* **19**, 191–210 (1993).

18. Mogi, M. et al. Experimental signature of the parity anomaly in a semi-magnetic topological insulator. *Nat. Phys.* **18**, 390-394 (2022).

19. Yang, F. et al. Dual-gated topological insulator thin-film device for efficient fermi-level tuning. *ACS Nano* **9**, 4050-4055 (2015).

20. Legg, H. F. *et al*. Giant magnetochiral anisotropy from quantum-confined surface states of topological insulator nanowires. *Nat. Nanotechnol.* **17**, 696–700 (2022).

21. Rößler, M. et al. Top-down fabrication of bulk-insulating topological insulator nanowires for quantum devices. *Nano Lett.* **23**, 2846-2853 (2023).

22. Ma, E. Y. *et al*. Unexpected edge conduction in mercury telluride quantum wells under broken time-reversal symmetry. *Nat. Commun.* **6**, 7252 (2015).

23. Maier, H. et al. Ballistic geometric resistance resonances in a single surface of a topological insulator. *Nat. Commun.* **8**, 2023 (2017).

24. Muranaka, S. *et al*. Anisotropic Wet Etching of WSe_2 and MoS_2 for Twist-Angle Extraction of Heterobilayers. *J. Phys. Chem. C* **128**, 7211–7215 (2024).

25. Munkhbat, B. *et al*. Transition metal dichalcogenide metamaterials with atomic precision. *Nat. Commun.* **11**, 4604 (2020).

26. He, T. *et al*. Etching Techniques in 2D Materials. *Adv. Mater. Technol.* **4**, 1900064 (2019).

27. Barton, A. et al. Impact of etch processes on the chemistry and surface states of the topological insulator Bi_2Se_3. *ACS Appl. Mater. Interfaces* **11**, 32144-32150 (2019).

28. Li, J. *et al*. Direct evidence of reactive ion etching induced damages in $Ge_2Sb_2Te_5$ based on different halogen plasmas. *Appl. Surf. Sci.* **378**, 163–166 (2016).

29. Sha, Y., Xiao, S., Zhang, X., Qin, F. & Gu, X. Layer-by-layer thinning of $MoSe_2$ by soft and reactive plasma etching. *Appl. Surf. Sci.* **411**, 182–188 (2017).

30. Xiao, S. *et al*. Atomic-layer soft plasma etching of MoS_2. *Sci. Rep.* **6**, 19945 (2016).

31. Kim, K. S. *et al.* Atomic Layer Etching Mechanism of MoS_2 for Nanodevices. *ACS Appl. Mater. Interfaces* **9**, 11967–11976 (2017).

32. Nipane, A. *et al.* Damage-Free Atomic Layer Etch of WSe_2: A Platform for Fabricating Clean Two-Dimensional Devices. *ACS Appl. Mater. Interfaces* **13**, 1930–1942 (2021).

33. Lin, T. *et al.* Controlled Layer-by-Layer Etching of MoS_2. *ACS Appl. Mater. Interfaces* **7**, 15892–15897 (2015).

34. Wang, Y. & Chhowalla, M. Making clean electrical contacts on 2D transition metal dichalcogenides. *Nat. Rev. Phys.* **4**, 101–112 (2022).

35. Bandyopadhyay, A. S., Saenz, G. A. & Kaul, A. B. Role of metal contacts and effect of annealing in high performance 2D WSe_2 field-effect transistors. *Surf. Coat. Technol.* **381**, 125084 (2020).

36. Allain, A., Kang, J., Banerjee, K. & Kis, A. Electrical contacts to two-dimensional semiconductors. *Nat. Mater.* **14**, 1195–1205 (2015).

37. Wang, Y. *et al.* Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature* **568**, 70–74 (2019).

38. Marinov, D. *et al.* Reactive plasma cleaning and restoration of transition metal dichalcogenide monolayers. *npj 2D Mater. Appl.* **5**, 1–10 (2021).

39. Sovizi, S. *et al.* Plasma Processing and Treatment of 2D Transition Metal Dichalcogenides: Tuning Properties and Defect Engineering. *Chem. Rev.* **123**, 13869–13951 (2023).

40. Tosun, M. *et al.* Air-Stable n-Doping of WSe_2 by Anion Vacancy Formation with Mild Plasma Treatment. *ACS Nano* **10**, 6853–6860 (2016).

41. Saifur, R. et al. Effect of physical vapor deposition on contacts to 2D MoS_2. *J. Appl. Phys.* **136**, 22 (2024).

42. Höflich, K. *et al.* Roadmap for focused ion beam technologies. *Appl. Phys. Rev.* **10**, 041311 (2023).

43. Sarcan, F. *et al.* Understanding the impact of heavy ions and tailoring the optical properties of large-area monolayer WS_2 using focused ion beam. *npj 2D Mater. Appl.* **7**, 1–7 (2023).

44. Friedensen, S., Mlack, J. T. & Drndić, M. Materials analysis and focused ion beam nanofabrication of topological insulator Bi_2Se_3. *Sci. Rep.* **7**, 13466 (2017).

45. Gracia-Abad, R., Sangiao, S., Kumar Chaluvadi, S., Orgiani, P. & Teresa, J. M. D. Ion-Induced Lateral Damage in the Focused Ion Beam Patterning of Topological Insulator Bi_2Se_3 Thin Films. *Materials* **16**, 2244 (2023).

46. Telkhozhayeva, M. Roadmap toward Controlled Ion Beam-Induced Defects in 2D Materials. *Adv. Funct. Mater.* **34**, 2404615 (2024).

47. Moll, Philip JW. Focused ion beam microstructuring of quantum matter." *Ann. Rev. Condens. Matter Phys.* **9**,147-162 (2018).